PY32MD320 Datasheet

32-bit ARM® Cortex®-M0+ Microcontroller

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Features

- Core
  - 32-bit ARM® Cortex®-M0+
  - Frequency up to 48 MHz
- Memories
  - 64 KB Flash memory
  - 8 KB SRAM
- Clock management
  - 4/8/16/22.12/24 MHz High-speed internal RC oscillator (HSI)
  - 32.768 kHz low-speed internal RC oscillator (LSI)
  - PLL (supports 2 multiplication of HSI)
- Power management and reset
  - Operating voltage: 2.0 to 5.5 V
  - Low-power modes: Sleep/Stop
  - Power-on/power-down reset (POR/PDR)
  - Brown-out reset (BOR)
  - Programmable voltage detector (PVD)
- General-purpose input and output (I/O)
  - Up to 14 I/Os, all available as external interrupts
- 3-channel DMA controller
- 1 x 12-bit ADC
  - Up to 7 external channels
  - Input voltage conversion range: 0 to V_{CC}
- Timers
  - 1 x 16-bit advanced-control timer (TIM1)
  - 4 x 16-bit general-purpose timers (TIM3/TIM14/TIM16/TIM17)
  - 1 x low-power timer (LPTIM), supporting wake-up from Stop mode
  - 1 x independent watchdog timer (IWDG)
  - 1 x window watchdog timer (WWDG)
  - 1 x SysTick timer
  - 1 x IRTIM
- RTC
- Communication interfaces
  - 2 x serial peripheral interfaces (SPI)
  - 2 x universal synchronous/asynchronous resceiver/transmitters (USART) with automatic baud rate detection
  - 1 x I^2C interface, supporting Standard mode (100 kHz) and Fast mode (400 kHz), with 7-bit addressing mode
- Hardware CRC-32 module
- 2 x comparators
- Built-in multi-function three-phase NN half-bridge pre-driver
  - Pre-driver max input voltage: 40 V
  - Recommended operating voltage: 5.5 to 18 V
  - Output current: ±0.8 A
  - Built-in bootstrap diode
  - LDO: 5 V/50 mA
  - 1 x programmable gain amplifier (PGA)
  - 4 x comparators (COMP) with adjustable voltage divider ratios
- Unique UID
- Serial wire debug (SWD)
- Operating temperature: -40 to 105 °C
- Packages: QFN32(4*4)

Content

1. Introduction

The PY32MD320 microcontrollers feature the high-performance 32-bit ARM® Cortex®-M0+ core operating at up to 48 MHz frequency, embed up to 64 KB Flash and 8 KB SRAM, and are available in multiple package options. The PY32MD320 integrates multi-channel I^2C, SPI, USART and other communication peripherals, one 12-bit ADC, five 16-bit timers, and two comparators.

The PY32MD320 microcontrollers operates across a temperature range of -40 to 105 °C and a voltage range of 2.0 to 5.5 V. It provides Sleep and Stop modes to meet the needs of different low-power applications.

The PY32MD320 microcontrollers are suitable for three-phase BLDC/PMSM. Common application scenarios are listed as follows: water pumps, power tools, model aircraft, etc.

Table 1-1 PY32MD320 series product features and peripheral counts

Peripherals		**PY32MD320K18U7**
Flash (KB)		64
SRAM (KB)		8
Timers	Advanced-control	1 (16-bit)
	General-purpose	4 (16-bit)
	Low power	1
	SysTick	1
	Watchdog	2
Comm. interfaces	SPI	2
	I^2C	1
	USART	2
DMA		3 ch
RTC		Yes
GPIOs		14
ADC (external + internal)		7+2
Comparators		2
Max. CPU frequency		48 MHz
Operating voltage		2.0 to 5.5 V
Operating temperature		-40 to 105 °C
Packages		QFN32(4*4)

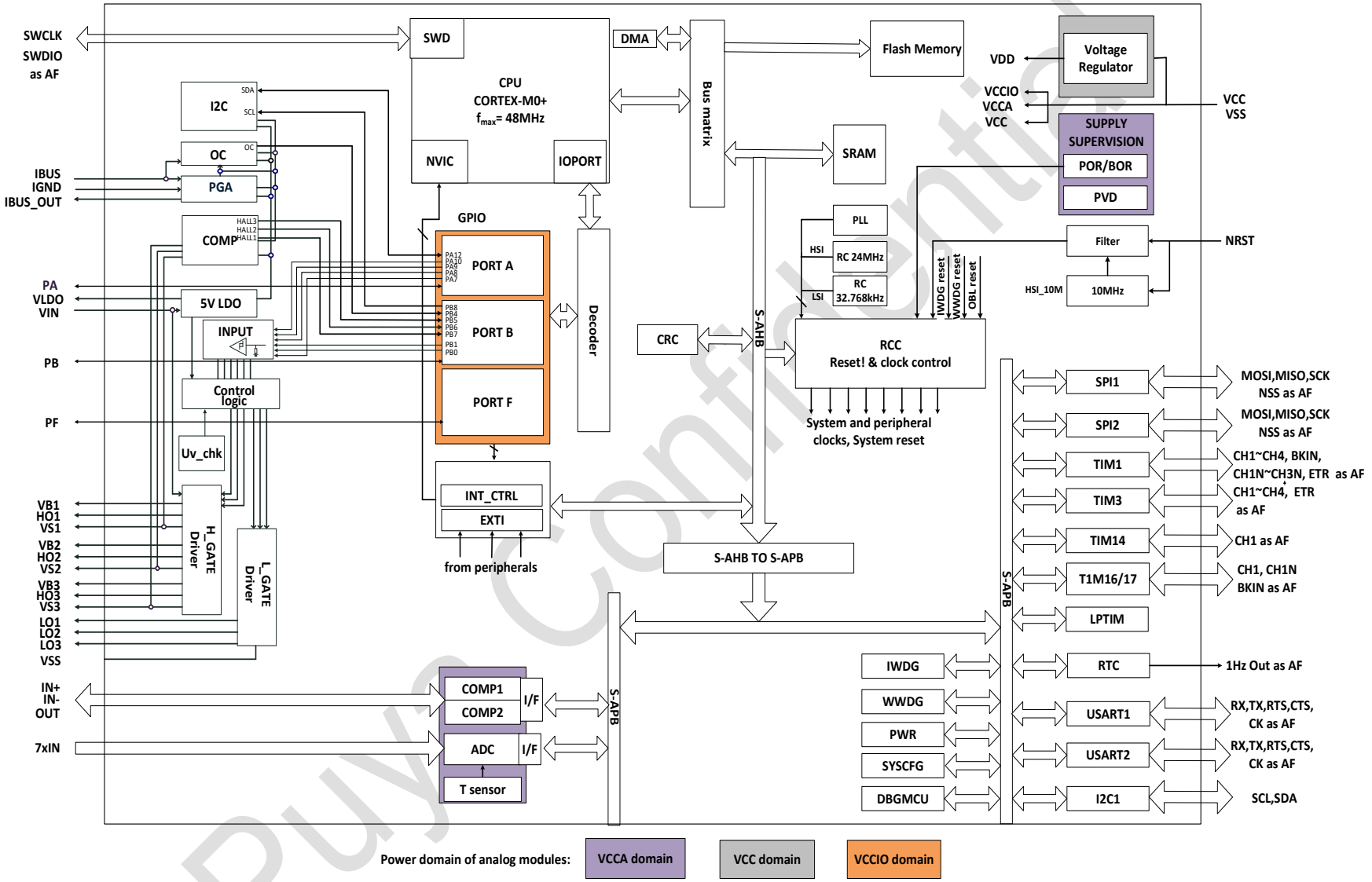


Figure 1-1 System block diagram

2. Functional overview

2.1. Arm® Cortex®-M0+ core

The Arm® Cortex®- M0+ is an Arm 32-bit Cortex processor designed for embedded applications. It provides developers with significant benefits, including:

- Simple architecture for easy learning and programming
- Ultra-low power consumption for energy-efficient operation
- Reduced code density

The Arm® Cortex®-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. It delivers high performance through a streamlined instruction set and hardware enhancements like a single-cycle multiplier, while achieving higher code density than other 8/16-bit MCUs.

The Arm® Cortex®-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC).

2.2. Memories

Embedded SRAM is accessed by byte (8 bits), half-word (16 bits) or word (32 bits).

The Flash memory is composed of two distinct physical areas:

- The Main flash area consists of application and user data
- 4 KB of Information area:
  - Option bytes
  - UID bytes
  - System memory

The protection of Main flash memory includes the following mechanisms:

- Read protection (RDP) prevents external access.
- Write protection (WRP) prevents unintended writes (caused by confusion of program). The minimum protection unit for write protection is 4 KB.
- Option byte write protection is a special design for unlock.

2.3. Clock management

After CPU startup, the default system clock frequency is HSI 8 MHz. The system clock frequency and system clock source can be reconfigured once the program is running. The frequency clocks that can be selected are:

- A 4/8/16/22.12/24 MHz internal high-precision HSI clock
- A 32.768 kHz configurable internal LSI clock
- PLL clock has HSI source.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. The maximum frequency of the AHB and the APB domains is 48 MHz.

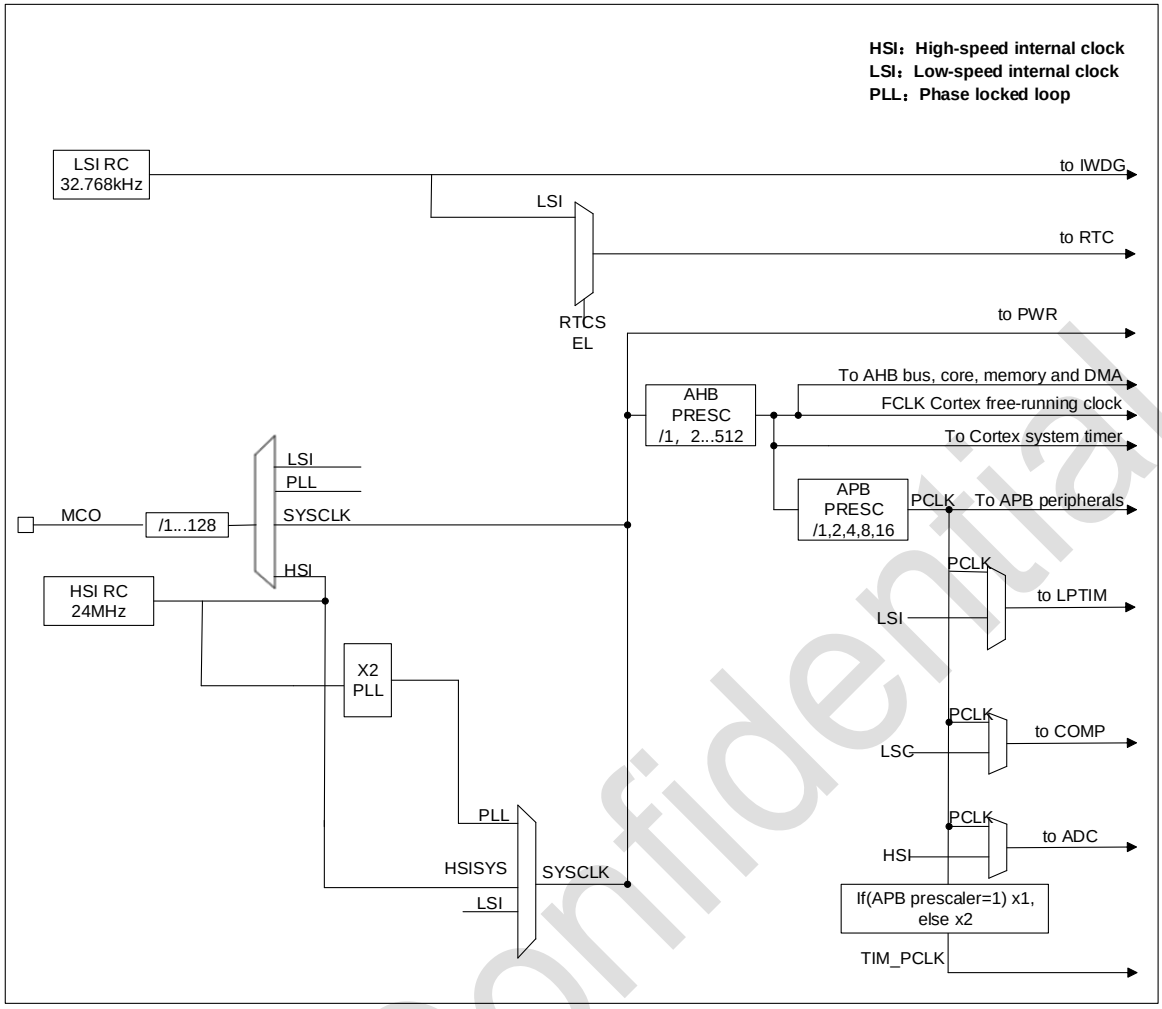


Figure 2-1 System clock structure diagram

2.4. Power management

2.4.1. Power block diagram

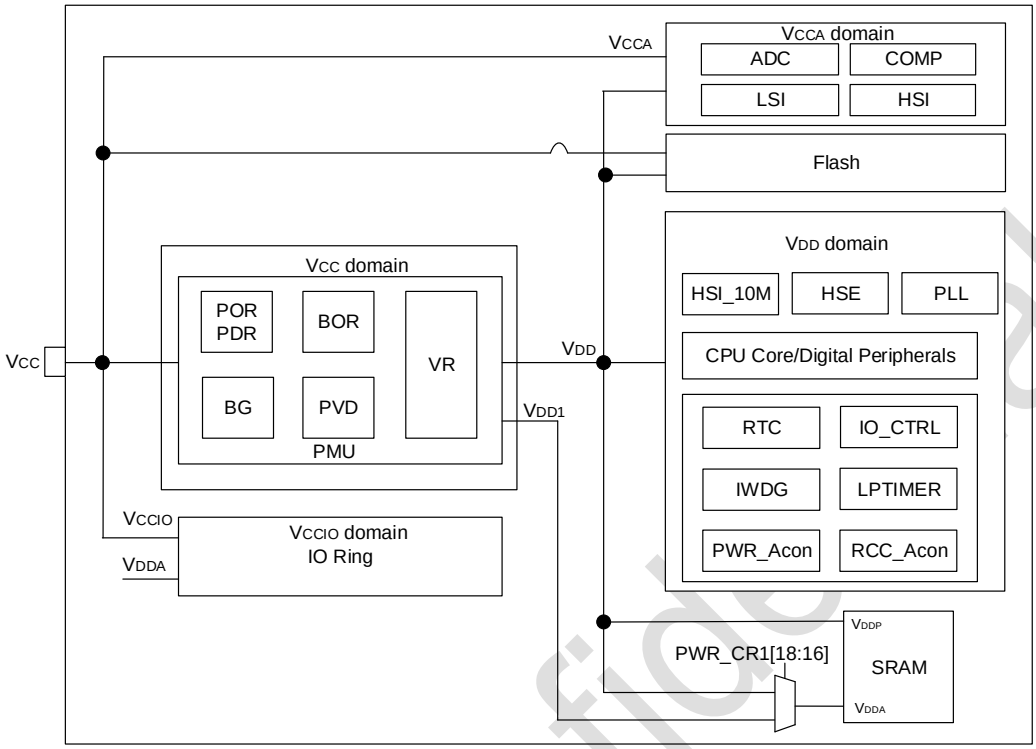


Figure 2-2 Power block diagram

Table 2-1 Power block diagram

No.	Power supply	Power value	Descriptions
1	V_{CC}	2.0 V to 5.5 V	The power is supplied to the chip through the power pins, with the power supply module comprising: Partial analog circuits.
2	V_{CCA}	2.0 V to 5.5 V	Powers for most analog modules, sourced from the V_{CC} PAD (a dedicated power PAD can also be designed separately).
3	V_{CCIO}	2.0 V to 5.5 V	Power to IO from V_{CC} PAD
4	V_{DD}	1.2 V/1.0 V±10%	VR supplies power to the main logic circuits and SRAM inside the chip. When the MR is powered, it outputs 1.2 V. According to the software configuration, when entering the Stop mode, it powered by MR or LPR, and the LPR output is determined by software.

2.4.2. Power monitoring

2.4.2.1. Power-on/power-down reset (POR/PDR)

The POR/PDR module, which provides power-on and power-down reset, remains active in all modes.

2.4.2.2. Brown-out reset (BOR)

In addition to POR/PDR, BOR (Brown-out reset) is also implemented. BOR can only be enabled and disabled through the option byte.

When the BOR is turned on, the BOR threshold can be selected by the option byte.

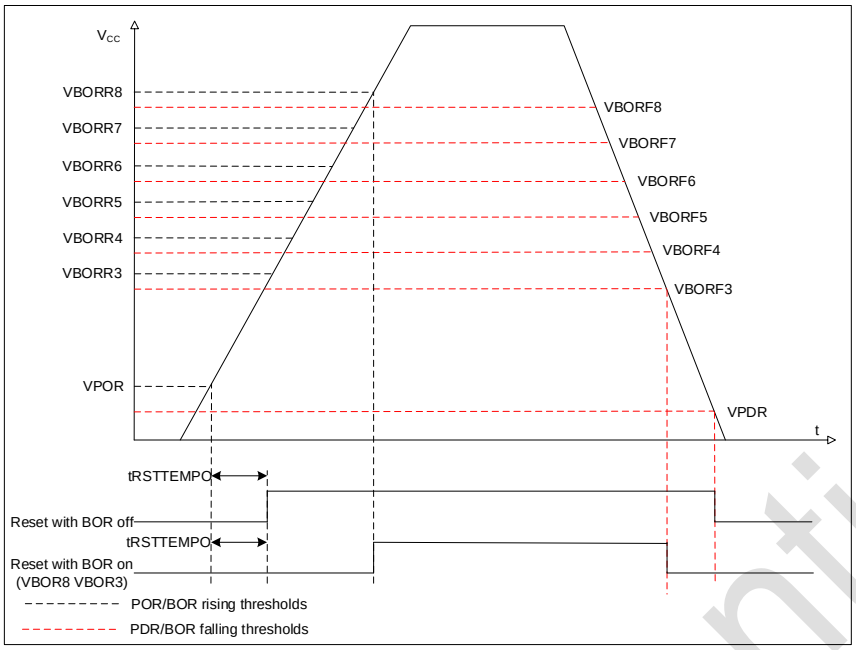


Figure 2-3 POR/PDR/BOR threshold

2.4.2.3. Programmable voltage detector (PVD)

Programmable voltage detector (PVD) module can be used to detect the V_{CC} power supply and the detection point is configured through the register. The device remains in reset mode when the monitored supply voltage V_{CC} is below a specified threshold.

This event is internally connected to line 16 of EXTI, depending on the rising/falling edge configuration of EXTI line 16, when V_{CC} rises above the detection point of PVD, or V_{CC} falls below the detection point of PVD, an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

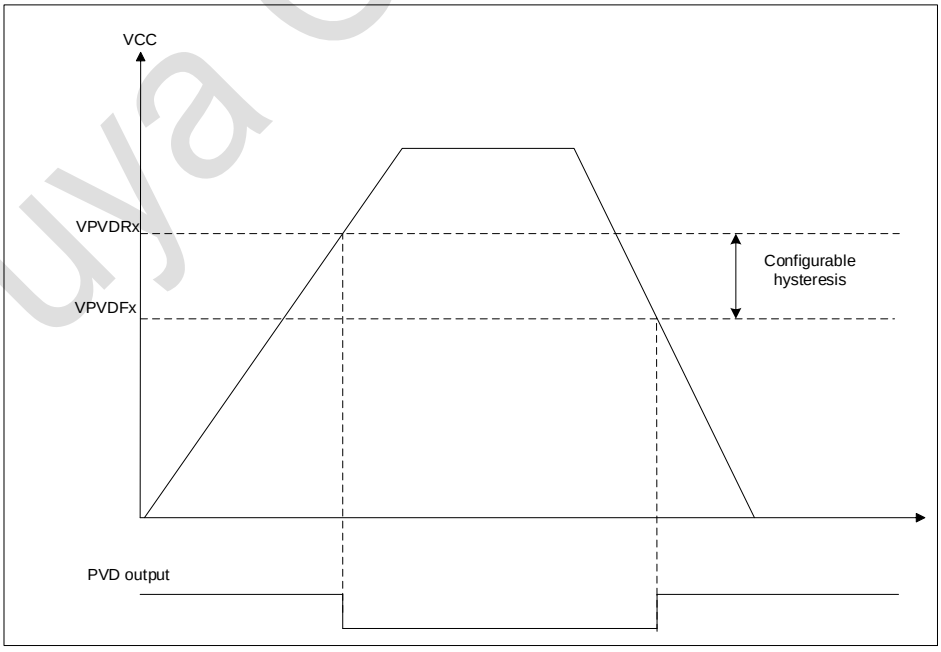


Figure 2-4 PVD threshold

2.4.3. Voltage regulator

The regulator has two operating modes:

- Main regulator (MR) is used in Run mode.
- Low power regulator (LPR) provides an option for even lower power consumption in Stop mode.

2.4.4. Low-power mode

In addition to the Run mode, the device has two low-power modes:

- **Sleep mode:** Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc. are operating). It is recommended to enable only essential modules and disable them after task completion.
- **Stop mode:** In this mode, SRAM and register contents are retained. PLL, HSI and HSE are turned off and most module clocks in the VDD domain are disabled. GPIO, PVD, COMP output, RTC, and LPTIM can wake up the Stop mode.

2.5. Reset

Two resets are designed in the chip: power reset and system reset.

2.5.1. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Brown-out reset (BOR)

2.5.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load (OBL) reset

2.6. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (floating, pull-up or pull-down and analog) or as peripheral alternate function. The I/O configuration can be locked.

2.7. DMA

Direct memory access (DMA) is used to provide a high-speed data transfer between peripherals and memory as well as from memory to memory.

The DMA controller have 3 channels in total, each one dedicated to manage memory access requests from one or more peripherals. The DMA controller includes an arbiter to handle DMA requests, which manages the priority of each DMA request.

DMA supports circular buffer management, eliminating the need for user code intervention when the controller reaches the end of the buffer.

Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.

DMA can be used for major peripherals: SPI, I^2C, USART, ADC and all TIMx timers (except TIM14 and LPTIM).

2.8. Interrupts and events

The PY32MD320 handles exceptions through the Cortex-M0+ processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

2.8.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a higher-priority interrupt event occurs and a lower-priority interrupt event is just waiting to be serviced, the later-arriving higher-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a higher-priority ISR and then starting a pending lower-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 interrupt priority
- Support 1 NMI
- Support 23 maskable external interrupts
- Support 6 Cortex-M0+ exceptions
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

2.8.2. Extended interrupt/event controller (EXTI)

EXTI adds flexibility to handle physical wire events and generates wake-up events when the processor wakes up from Stop mode.

The EXTI controller has multiple channels, including up to 16 GPIOs, 1 PVD output, 2 COMP outputs, as well as RTC and LPTIM Wake-up signals. GPIO, PVD and COMP can be configured to be

triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 to 15 channel through the select signal.

- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.
- Registers in the EXTI controller latch each event. Even in Stop mode, after the processor wakes up from Stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.9. Analog-to-digital converter (ADC)

The device has a 12-bit SAR-ADC. The module has a total of up to 9 channels to be measured, including 7 external and 2 internal channels.

A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.

The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.

An efficient low-power mode is implemented to allow very low consumption at low frequency.

Interrupt generation at ADC ready, the end of sampling, the end of conversion, end of sequence conversion, analog watchdog or overrun events

2.10. Comparators (COMP)

General purpose comparators are integrated, which can be used in combination with timer. Comparators can be used as:

- Triggered by analog signal to wake-up function from low-power mode
- Analog signal conditioning
- Cycle by cycle current control loop when comparators are connected with PWM output from timer

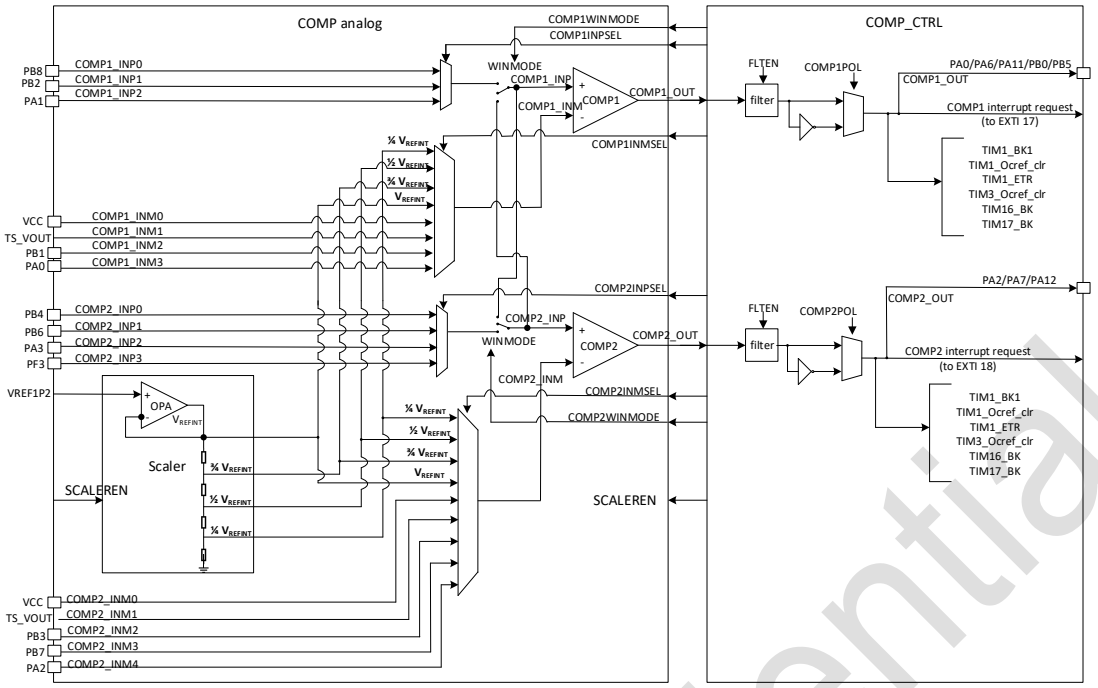


Figure 2-5 COMP block diagram

2.10.1. COMP main features

- Each comparator has configurable positive or negative input for flexible voltage selection:
  - Multiple I/O pins
  - Power supply V_{CC}
  - Temperature sensor output
  - Power supply V_{CC} and 3 fractional values provided by voltage division (1/4, 1/2 and 3/4).
- Configurable hysteresis function
- Programmable speed and consumption
- The output can be triggered by a connection to the I/O or timer input
  - OCREF_CLR event (cycle-by-cycle current control)
  - Brakes for fast PWM shutdown

Each COMP has interrupt generation capability and is used to wake up the device from low power mode (Sleep/Stop) (via EXTI)

2.11. Timers

The different timers feature as blow:

Table 2-2 Timer characteristics

Type	Timer	Counter resolution	Counter type	Prescaler	DMA	Capture/compare channels	Comple-mentary outputs
Advanced-control	TIM1	16-bit	up,down up/down	1 to 65536	Yes	4	3
General-purpose	TIM3	16-bit	up,down up/down	1 to 65536	Yes	4	-
	TIM14	16-bit	up	1 to 65536	-	1	-
	TIM16,TIM17	16-bit	up	1 to 65536	Yes	1	1

2.11.1. Advanced-control timer

The advanced-control timer (TIM1) is consist of a 16-bit auto-reload counter driven by a programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, TIM1/TIM8 have full modulation capability (0 to 100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the Timer Link feature for synchronization or event chaining.

TIM1 supports the DMA function.

2.11.2. General-purpose timers

2.11.2.1. TIM3

- The TIM3 general-purpose timer consists of a 16-bit auto-reload counter driven by a 16-bit programmable prescaler. There are four independent channels each for input capture/output compare, PWM or one-pulse mode output.
- TIM3 can work with the TIM1 by the Timer Link.
- TIM3 supports the DMA function.
- This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.
- The counter can be frozen in debug mode.

2.11.2.2. TIM14

- The general-purpose timer TIM14 is consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM14 features two single channel for input capture/output compare, PWM or one-pulse mode output.
- The counter can be frozen in debug mode.

2.11.2.3. TIM16/TIM17

- TIM16 and TIM17 consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM16/TIM17 features one single channel for input capture/output compare, PWM or one-pulse mode output.

- TIM16/TIM17 have complementary outputs with dead time.
- TIM16/TIM17 supports DMA function.
- The counter can be frozen in debug mode.

2.11.3. Low power timer

- LPTIM is a 16 -bit upcounter with a 3-bit prescaler and support a single count.
- LPTIM can be configured as a Stop mode wake-up source.
- The counter can be frozen in debug mode.

2.11.4. IWDG

- Independent watchdog (IWDG) is integrated in the chip, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.
- The IWDG is clocked by LSI, so even if the main clock fails, it can keep working.
- IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.
- The IWDG hardware mode can be enabled by option byte.
- IWDG is the wake-up source of Stop mode, which wakes up Stop mode by reset.
- The counter can be frozen in debug mode.

2.11.5. WWDG

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in debug mode.

2.11.6. SysTick timer

SysTick timer is dedicated to real-time operating systems (RTOS), but could also be used as a standard down counter.

SysTick features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.12. Real-time clock (RTC)

The RTC is an independent counter. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.

- RTC is a 32-bit programmable counter with a prescaler factor of up to 2^{20} bits.
- RTC counter clock source can be LSI and the stop wake-up source.
- RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).

- RTC supports clock calibration.
- RTC can be frozen in debug mode.

2.13. Inter-integrated circuit interface (I^2C)

The Inter-integrated circuit (I^2C) bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing. It supports Standard mode (Sm) and Fast mode (Fm) .

I^2C features:

- Support Slave and Master mode
  - Support different communication speeds
  - Standard mode (Sm): up to 100 kHz
  - Fast Mode (Fm): up to 400 kHz
- As Master
  - Generate clock
  - Generation of start and stop
- As Slave
  - Programmable I^2C address detection
  - Discovery of the STOP bit
- 7-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I^2C busy flag bit
- Error flag
  - Master arbitration loss
  - ACK failure after address/data transfer
  - Start/Stop error
  - Overrun/Underrun (clock stretching function disable)
- Optional clock stretching
- Single-byte buffer with DMA capability
- Software reset
- Analog noise filter function

2.14. Universal synchronous/asynchronous receiver/transmitter (USART)

The PY32MD320 contains two USARTs, and the two function exactly the same.

The USARTs provide a flexible method for full-duplex data exchange with external devices using the

industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baud rate generator to provide a wide range of baud rate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baud rate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USART features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baud rate shared by transmit and receive
- Automatic baud rate detection
- Programmable data length of 8 or 9 bits
- Configurable STOP bit (1 or 2 bits)
- Synchronous mode and clock output function for synchronous communication
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control
- Receive/transmit bytes by DMA buffer
- Transfer detection flag
  - Receive buffer full
  - Send empty buffer
  - End of transmission flags
- Parity control
  - Transmit parity bit
  - Check the received data byte
- Flagged interrupt sources
  - CTS change
  - Transmit data register empty
  - Transmission complete
  - Receive full data register
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation

  - Detection error
- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection

2.15. Serial peripheral interface (SPI)

PY32MD320 contains 2 SPIs.

The serial peripheral interface (SPI) protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices. This interface can be configured in Master mode and provides the serial clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or Slave mode
- 3-wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- Master mode frequency up to $f_{PCLK}/4$
- Slave mode frequency up to $f_{PCLK}/4$
- Both Master and Slave modes can be managed by software or hardware NSS: dynamic change of Master/Slave operating mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Motorola mode
- Interrupt-causing Master mode faults or overloads
- Two 32-bit Rx and Tx FIFOs with DMA capability

2.16. SWD

An ARM SWD interface allows serial debugging tools to be connected to the PY32MD320.

3. Pinouts and pin descriptions

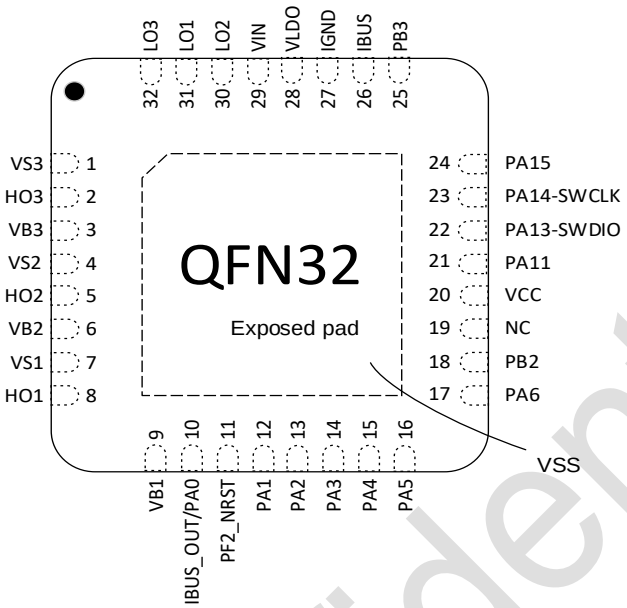


Figure 3-1 QFN32(4*4) Pinout1 PY32MD320K1xU7 (Top view)

Table 3-1 Legend/abbreviations used in the pinout table

Type		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		I/O	Input/output pin
		NC	No internal connection
I/O structure		COM	Standard 5 V I/O, supporting analog input/output functions
		NRST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		-	Unless otherwise specified, all ports are used as analog inputs between and after reset
Pin functions	Alternate functions	-	Function selected through GPIOx_AFR register
	Additional functions	-	Functions directly selected/enabled through peripheral registers

Table 3-2 Legend/abbreviations used for the Gate Driver pin definitions

Packages	Pin name	Pin function
QFN32(4*4) K1		
1	VS3	Channel 3 low-side gate driver output
2	HO3	Channel 3 high-side gate driver output
3	VB3	Channel 3 high-side floating power supply
4	VS2	Channel 2 high-side floating reference ground
5	HO2	Channel 2 high-side gate driver output
6	VB2	Channel 2 high-side floating power supply
7	VS1	Channel 1 high-side floating reference ground
8	HO1	Channel 1 high-side gate driver output
9	VB1	Channel 1 high-side floating power supply
10	IBUS_OUT	Motor bus current signal output
26	IBUS	Motor bus current sampling input
27	IGND	Motor current sampling reference ground input
28	VLDO	LDO output voltage
29	VIN	Driver power supply input
30	LO2	Channel 2 low-side gate driver output
31	LO1	Channel 1 low-side gate driver output
32	LO3	Channel 3 low-side gate driver output

Table 3-3 QFN32 pin definitions

Packages	IO	Driver	Pin type	I/O structure	Pin functions		
QFN32(4*4) K1					Notes	Alternate functions	Additional functions
1	-	VS3	-	-		-	-
2	PB1	HO3	-	-		TIM1_CH3N	-
3	-	VB3	-	-		-	-
4	-	VS2	-	-		-	-
5	PB0	HO2	-	-		TIM1_CH2N	-
6	-	VB2	-	-		-	-
7	-	VS1	-	-		-	-
8	PA7	HO1	-	-		TIM1_CH1N	-
9	-	VB1	-	-		-	-
10	PA0	IBUS_OUT	-	-		-	-
11	PF2-NRST	-	I/O	NRST	(1)	MCO	NRST
						SPI2_MOSI	
						USART2_RX	
10	PA0	-	I/O	COM		SPI2_SCK	ADC_IN0COMP1_INM
						USART1_CTS	
						USART2_CTS	
						COMP1_OUT	
						TIM1_CH3	
						TIM1_CH1N	
						SPI1_MISO	
						USART2_TX	
						IR_OUT	
12	PA1	-	I/O	COM		SPI1_SCK	COMP1_INP ADC_IN1
						USART1_RTS	
						USART2_RTS	
						EVENTOUT	
						SPI1_MOSI	
						USART2_RX	
						TIM1_CH4	
						TIM1_CH2N	
						MCO	
13	PA2	-	I/O	COM		SPI1_MOSI	COMP2_INM ADC_IN2
						USART1_TX	
						USART2_TX	
						COMP2_OUT	
						SPI1_SCK	
						TIM3_CH1	
						I^2C_SDA	
14	PA3	-	I/O	COM		SPI2_MISO	COMP2_INP ADC_IN3
						USART1_RX	

Packages	IO	Driver	Pin type	I/O structure	Pin functions		
QFN32(4*4) K1					Notes	Alternate functions	Additional functions
						USART2_RX	
						EVENTOUT	
						SPI1_MOSI	
						TIM1_CH1	
						I^2C_SCL	
15	PA4	-	I/O	COM		SPI1_NSS	ADC_IN4
						USART1_CK	
						SPI2_MOSI	
						TIM14_CH1	
						USART2_CK	
						ENENTOUT	
						RTC_OUT	
						TIM3_CH3	
						USART2_TX	
16	PA5	-	I/O	COM		SPI1_SCK	ADC_IN5
						LPTIM_ETR	
						EVENTOUT	
						TIM3_CH2	
						USART2_RX	
						MCO	
17	PA6	-	I/O	COM		SPI1_MISO	ADC_IN6
						TIM3_CH1	
						TIM1_BKIN	
						TIM16_CH1	
						COMP1_OUT	
						USART1_CK	
						RTC_OUT	
19	NC	-	NC				
18	PB2	-	I/O	COM		USART1_RX	COMP1_INP
						USART2_RX	
						SPI2_SCK	
20	V_{CC}	-	S	-		Digital power supply	
21	PA11	-	I/O	COM		SPI1_MISO	-
						USART1_CTS	
						TIM1_CH4	
						EVENTOUT	
						USART2_CTS	
						I^2C_SCL	
						COMP1_OUT	
22	PA13(SWDIO)	-	I/O	COM	(2)	SWDIO	-
						IR_OUT	

Packages	IO	Driver	Pin type	I/O structure	Pin functions		
QFN32(4*4) K1					Notes	Alternate functions	Additional functions
						EVENTOUT	
						SPI1_MISO	
						TIM1_CH2	
						USART1_RX	
						MCO	
23	PA14(SWCLK)	-	I/O	COM	(2)	SWCLK	-
						USART1_TX	
						USART2_TX	
						EVENTOUT	
						MCO	
24	PA15	-	I/O	COM		SPI1_NSS	-
						USART1_RX	
						USART2_RX	
						EVENTOUT	
25	PB3	-	I/O	COM		SPI1_SCK	COMP2_INM
						TIM1_CH2	
						USART1_RTS	
						USART2_RTS	
						EVENTOUT	
Exposed pad	VSS	-	S	-		Ground	
26	-	IBUS	-	-		-	-
27	-	IGND	-	-		-	-
28	-	VLDO	-	-		-	-
29	-	VIN	-	-		-	-
30	PA9	LO2	-	-		TIM1_CH2	-
31	PA8	LO1	-	-		TIM1_CH1	-
32	PA10	LO3	-	-		TIM1_CH3	-

1. Configured by option bytes to choose PF2 or NRST.
2. After reset, PA13 and PA14 are configured as SWDIO AF and SWCLK functions, the former has an internal pull-up resistor and the latter has an internal pull-down resistor activated.

3.1. Alternate functions selected through GPIOA_AFR registers for port A

Table 3-2 Port A alternate functions mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI2_SCK	USART1_CTS	-	-	USART2_CTS	-	-	COMP1_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_TX	SPI1_MISO	-	-	TIM1_CH3	TIM1_CH1N	IR_OUT
PA1	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_SCK	USART1_RTS	-	-	USART2_RTS	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_RX	SPI1_MOSI	-	-	TIM1_CH4	TIM1_CH2N	MCO
PA2	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	USART1_TX	-	-	USART2_TX	-	-	COMP2_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	SPI1_SCK	-	I^2C_SDA	TIM3_CH1	-	-
PA3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI2_MISO	USART1_RX	-	-	USART2_RX	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	SPI1_MOSI	-	I^2C_SCL	TIM1_CH1	-	-
PA4	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_NSS	USART1_CK	SPI2_MOSI	-	TIM14_CH1	USART2_CK	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_TX	-	-	-	TIM3_CH3	-	RTC_OUT
PA5	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_SCK	-	-	-	-	LPTIM1_ETR	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_RX	-	-	-	TIM3_CH2	-	MCO
PA6	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	-	COMP1_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_CK	-	-	-	-	-	-	RTC_OUT
PA7	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	USART2_TX	SPI1_MISO	-	I^2C_SDA	-	-	-
PA8	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI2_NSS	USART1_CK	TIM1_CH1	-	USART2_CK	MCO	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	USART2_RX	SPI1_MOSI	-	I^2C_SCL	-	-	-
PA9	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**

	SPI2_MISO	USART1_TX	TIM1_CH2	-	USART2_TX	MCO	I²C_SCL	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	-	SPI1_SCK	-	I²C_SDA	TIM1_BKIN	-	-
PA10	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI2_MOSI	USART1_RX	TIM1_CH3	-	USART2_RX	TIM17_BKIN	I²C_SDA	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	-	SPI1_NSS	-	I²C_SCL	-	-	-
PA11	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MISO	USART1_CTS	TIM1_CH4	-	USART2_CTS	EVENTOUT	I²C_SCL	COMP1_OUT
PA12	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	USART1_RTS	TIM1_ETR	-	USART2_RTS	EVENTOUT	I²C_SDA	COMP2_OUT
PA13	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SWDIO	IR_OUT	-	-	-	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	-	SPI1_MISO	-	-	TIM1_CH2	-	MCO
PA14	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SWCLK	USART1_TX	-	-	USART2_TX	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	-	-	-	-	-	MCO
PA15	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_NSS	USART1_RX	-	-	USART2_RX	-	-	EVENTOUT

3.2. Alternate functions selected through GPIOB_AFR registers for port B

Table 3-3 Port B alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	SPI1_NSS	TIM3_CH3	TIM1_CH2N	-	-	EVENTOUT	-	COMP1_OUT
PB1	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	-	-	EVENTOUT
PB2	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_RX	SPI2_SCK	-	USART2_RX	-	-	-	-
PB3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_SCK	TIM1_CH2	-	USART1_RTS	USART2_RTS	-	-	EVENTOUT
PB4	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MISO	TIM3_CH1	-	USART1_CTS	USART2_CTS	TIM17_BKIN	-	EVENTOUT
PB5	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	USART1_CK	USART2_CK	LPTIM_IN1	-	COMP1_OUT
PB6	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_TX	TIM1_CH3	TIM16_CH1N	SPI2_MISO	USART2_TX	LPTIM_ETR	I^2C_SCL	EVENTOUT
PB7	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_RX	SPI2_MOSI	TIM17_CH1N	-	USART2_RX	-	I^2C_SDA	EVENTOUT
PB8	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	SPI2_SCK	TIM16_CH1	-	USART2_TX	-	I^2C_SCL	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	-	-	SPI2_NSS	I^2C_SDA	TIM17_CH1	-	IR_OUT

3.3. Alternate functions selected through GPIOF_AFR registers for port F

Table 3-4 Port F alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0-OSC_IN	-	-	TIM14_CH1	SPI2_SCK	USART2_RX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	USART2_TX	-	-	I^2C_SDA	-	-	-
PF1_OSC_OUT	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	-	SPI2_MISO	USART2_TX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	USART2_RX	SPI1_NSS	-	I^2C_SCL	TIM14_CH1	-	-
PF2-NRST	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	-	SPI2_MOSI	USART2_RX	-	MCO	-
PF3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_TX	-	-	SPI2_MISO	USART2_TX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	SPI1_NSS	-	-	TIM3_CH3	-	RTC_OUT
PF4	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	-	-	-	-	-	-

4. Memory mapping

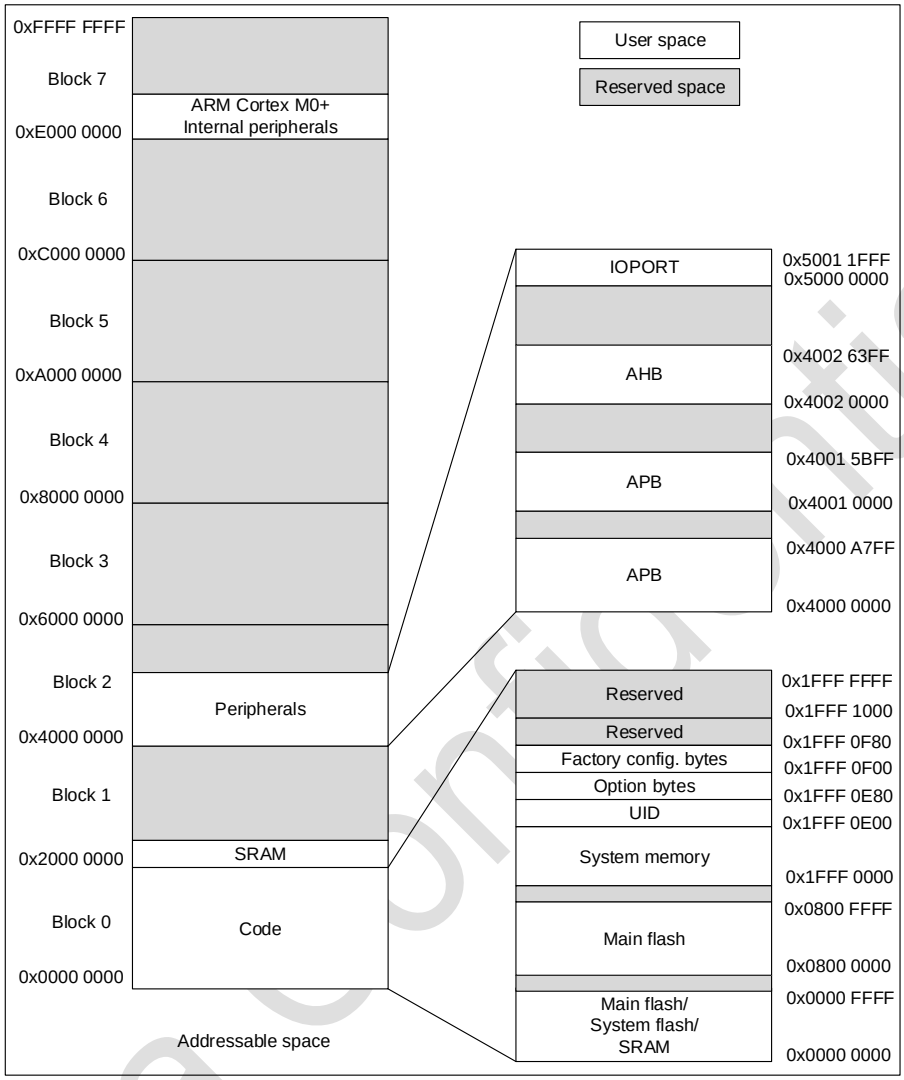


Figure 4-1 Memory mapping

Table 4-1 Memory boundary address

Type	Boundary Address	Size	Memory area	Description
SRAM	0x2000 2000-0x3FFF FFFF	-	Reserved	-
	0x2000 0000-0x2000 1FFF	8 KB	SRAM	SRAM up to 8 KB depending on hard-ware
Code	0x1FFF 0F80-0x1FFF 0FFF	-	Reserved	-
	0x1FFF 0F00-0x1FFF 0F7F	128 bytes	Factory config. bytes	HSI trimming data, Flash erase/write time configuration parameters
	0x1FFF 0E80-0x1FFF 0EFF	128 bytes	Option bytes	option bytes
	0x1FFF 0E00-0x1FFF 0E7F	128 bytes	UID	Unique ID
	0x1FFF 0000-0x1FFF 0DFF	-	Reserved	-
	0x0801 0000-0x1FFF FFFF	-	Reserved	-
	0x0800 0000-0x0800 FFFF	64 KB	Main flash memory	-
	0x0001 0000-0x07FF FFFF	-	Reserved	-

Type	Boundary Address	Size	Memory area	Description
	0x0000 0000-0x0000 FFFF	64 KB	Main flash memory	-

Table 4-2 Peripheral register address

Bus	Boundary Address	Size	Peripheral
-	0xE000 0000-0xE00F FFFF	-	M0+
IOPORT	0x5000 1800-0x5FFF FFFF	-	Reserved
	0x5000 1400-0x5000 17FF	1 KB	GPIOF
	0x5000 0800-0x5000 13FF	-	Reserved
	0x5000 0400-0x5000 07FF	1 KB	GPIOB
	0x5000 0000-0x5000 03FF	1 KB	GPIOA
AHB	0x4002 3400-0x4FFF FFFF	-	Reserved
	0x4002 300C-0x4002 33FF	1 KB	Reserved
	0x4002 3000-0x4002 3008		CRC
	0x4002 2400-0x4002 2FFF	-	Reserved
	0x4002 2124-0x4002 23FF	1 KB	Reserved
	0x4002 2000-0x4002 2120		Flash
	0x4002 1C00-0x4002 1FFF	-	Reserved
	0x4002 1888-0x4002 1BFF	1 KB	Reserved
	0x4002 1800-0x4002 1884		EXTI
	0x4002 1400-0x4002 17FF	-	Reserved
	0x4002 1064-0x4002 13FF	1 KB	Reserved
	0x4002 1000-0x4002 1060		RCC
	0x4002 0C00-0x4002 0FFF	-	Reserved
	0x4002 0040-0x4002 03FF	1 KB	Reserved
	0x4002 0000-0x4002 003C		DMA
APB	0x4001 5C00-0x4001 FFFF	-	Reserved
	0x4001 5880-0x4001 5BFF	1 KB	Reserved
	0x4001 5800-0x4001 587F		DBG
	0x4001 4C00-0x4001 57FF	-	Reserved
	0x4001 4850-0x4001 4BFF	1 KB	Reserved
	0x4001 4800-0x4001 484C		TIM17
	0x4001 4450-0x4001 47FF	1 KB	Reserved
	0x4001 4400-0x4001 404C		TIM16
	0x4001 3C00-0x4001 43FF	-	Reserved
	0x4001 381C-0x4001 3BFF	1 KB	Reserved
	0x4001 3800-0x4001 3018		USART1
	0x4001 3400-0x4001 37FF	-	Reserved
	0x4001 3010-0x4001 33FF	1 KB	Reserved
	0x4001 3000-0x4001 300C		SPI1
	0x4001 2C50-0x4001 2FFF	1 KB	Reserved
	0x4001 2C00-0x4001 2C4C		TIM1

Bus	Boundary Address	Size	Peripheral
	0x4001 2800-0x4001 2BFF	-	Reserved
	0x4001 270C-0x4001 27FF	1 KB	Reserved
	0x4001 2400-0x4001 2708		ADC
	0x4001 0400-0x4001 23FF	-	Reserved
	0x4001 0220-0x4001 03FF	1 KB	Reserved
	0x4001 0200-0x4001 021F		COMP1 and COMP2
	0x4001 0000-0x4001 01FF		SYSCFG
	0x4000 8000-0x4000 FFFF	-	Reserved
	0x4000 7C28-0x4000 7FFF	1 KB	Reserved
	0x4000 7C00-0x4000 7C24		LPTIM
	0x4000 7400-0x4000 7BFF	-	Reserved
	0x4000 7018-0x4000 73FF	1 KB	Reserved
	0x4000 7000-0x4000 7014		PWR
	0x4000 5800-0x4000 6FFF	-	Reserved
	0x4000 5434-0x4000 57FF	1 KB	Reserved
	0x4000 5400-0x4000 5430		I^2C
	0x4000 4800-0x4000 53FF	3 KB	Reserved
	0x4000 441C-0x4000 47FF	1 KB	Reserved
	0x4000 4400-0x4000 4418		USART2
	0x4000 3C00-0x4000 43FF	-	Reserved
	0x4000 3810-0x4000 3BFF	1 KB	Reserved
	0x4000 3800-0x4000 380C		SPI2
	0x4000 3400-0x4000 37FF	-	Reserved
	0x4000 3014-0x4000 33FF	1 KB	Reserved
	0x4000 3000-0x4000 0010		IWDG
	0x4000 2C0C-0x4000 2FFF	1 KB	Reserved
	0x4000 2C00-0x4000 2C08		WWDG
	0x4000 2830-0x4000 2BFF	1 KB	Reserved
	0x4000 2800-0x4000 282C		RTC
	0x4000 2420-0x4000 27FF	-	Reserved
	0x4000 2400-0x4000 241C		Reserved
	0x4000 2054-0x4000 23FF	1 KB	Reserved
	0x4000 2000-0x4000 0050		TIM14
	0x4000 0800-0x4000 1FFF	-	Reserved
	0x4000 0450-0x4000 07FF	1 KB	Reserved
	0x4000 0400-0x4000 044C		TIM3
	0x4000 0000-0x4000 03FF	-	Reserved

5. Electrical characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1. Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at T_A = 25 °C and $T_A = T_{A(max)}$ (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2. Typical values

Unless otherwise specified, typical data is based on T_A = 25°C and V_{CC} = 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated.

5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics(1)

Symbol	Descriptions	Min	Max	Unit
V_{CC}	External mains power supply	-0.3	6.25	V
V_{IN}	Input voltage of other pins	-0.3	V_{CC}+0.3	V

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.

Table 5-2 Current characteristics

Symbol	Descriptions	Max	Unit
I_{VCC}	Total current into V_{CC} pin (supply current)(1)	100	mA
I_{VSS}	Total current flowing out of the V_{SS} pin (sink current)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any COM I/O and control pin(2)	20	
	Total output current sourced by sum of all I/Os and control pins	-20	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. These I/O types refer to the terms and symbols defined by pins.

Table 5-3 Thermal characteristics

Symbol	Descriptions	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	℃
T_J	Maximum junction temperature	150	℃

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	MHz
V_{CC}	Standard operating voltage	-	2.0	5.5	V
V_{IN}	I/O input voltage	-	-0.3	V_{CC}+0.3	V
T_A	Ambient temperature	-	-40	105	℃
T_J	Junction temperature	-	-40	125	℃

5.3.2. Operating conditions at power-on/power-down

Table 5-5 Operating conditions at power-on/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VCC}	V_{CC} rise rate	-	10	∞	μs/V
	V_{CC} fall rate	-	20	∞	

5.3.3. Embedded reset and PVD module characteristics

Table 5-6 Embedded reset characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization	-	-	4.0	7.5	ms
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	1.50(2)	1.60	1.70	V
		Falling edge	1.45(1)	1.55	1.65(2)	
V_{BOR1}	BOR1 threshold	Rising edge	Reserved			V
		Falling edge				
V_{BOR2}	BOR2 threshold	Rising edge				V
		Falling edge				
V_{BOR3}	BOR3 threshold	Rising edge	2.10(2)	2.20	2.30	V
		Falling edge	2.00	2.10	2.20(2)	
V_{BOR4}	BOR4 threshold	Rising edge	2.30(2)	2.40	2.50	V
		Falling edge	2.20	2.30	2.40(2)	
V_{BOR5}	BOR5 threshold	Rising edge	2.50(2)	2.60	2.70	V
		Falling edge	2.40	2.50	2.60(2)	
V_{BOR6}	BOR6 threshold	Rising edge	2.70(2)	2.80	2.90	V
		Falling edge	2.60	2.70	2.80(2)	
V_{BOR7}	BOR7 threshold	Rising edge	2.90(2)	3.00	3.10	V
		Falling edge	2.80	2.90	3.00(2)	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR8}	BOR8 threshold	Rising edge	3.10(2)	3.20	3.30	V
		Falling edge	3.00	3.10	3.20(2)	
V_{PVD0}	PVD0 threshold	Rising edge	Reserved			V
		Falling edge				
V_{PVD1}	PVD1 threshold	Rising edge				V
		Falling edge				
V_{PVD2}	PVD2 threshold	Rising edge	2.10(2)	2.20	2.30	V
		Falling edge	2.00	2.10	2.20(2)	
V_{PVD3}	PVD3 threshold	Rising edge	2.30(2)	2.40	2.50	V
		Falling edge	2.20	2.30	2.40(2)	
V_{PVD4}	PVD4 threshold	Rising edge	2.50(2)	2.60	2.70	V
		Falling edge	2.40	2.50	2.60(2)	
V_{PVD5}	PVD5 threshold	Rising edge	2.70(2)	2.80	2.90	V
		Falling edge	2.60	2.70	2.80(2)	
V_{PVD6}	PVD6 threshold	Rising edge	2.90(2)	3.00	3.10	V
		Falling edge	2.80	2.90	3.00(2)	
V_{PVD7}	PVD7 threshold	Rising edge	3.10(2)	3.20	3.30	V
		Falling edge	3.00	3.10	3.20(2)	
$V_{POR\_PDR\_hyst}$(1)	POR/PDR hysteresis	-	-	50	-	mV
$V_{PVD\_BOR\_hyst}$(1)	PVD hysteresis	-	-	100	-	mV
$I_{CC(PVD)}$	PVD power consumption	-	-	0.6	-	μA
$I_{CC(BOR)}$	BOR consumption	-	-	0.6	-	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.4. Supply current characteristics

Table 5-7 Current consumption in Run mode

Symbol	Conditions						Typ(1)	Max	Unit
	System clock	Frequency	Code	Run	Peripheral Clock	Flash sleep			
$I_{CC(Run)}$	HSI	48 MHz	While(1)	Flash	ON	DISABLE	2.6	-	mA
					OFF	DISABLE	1.7	-	
		24 MHz			ON	DISABLE	1.5	-	
					OFF	DISABLE	0.9	-	
		16 MHz			ON	DISABLE	1.1	-	
					OFF	DISABLE	0.7	-	
		8 MHz			ON	DISABLE	0.7	-	
					OFF	DISABLE	0.5	-	
		4 MHz			ON	DISABLE	0.5	-	
					OFF	DISABLE	0.35	-	
	LSI	32.768 kHz			ON	DISABLE	170	-	μA

Symbol	Conditions						Typ(1)	Max	Unit
	System clock	Frequency	Code	Run	Peripheral Clock	Flash sleep			
					OFF	DISABLE	170	-	
		32.768 kHz			ON	ENABLE	95	-	
					OFF	ENABLE	95	-	

1. Data based on characterization results, not tested in production.

Table 5-8 Current consumption in Sleep mode

Symbol	Conditions				Typ(1)	Max	Unit
	System clock	Frequency	Peripheral Clock	Flash sleep			
I_{CC}(sleep)	HSI	48 MHz	ON	DISABLE	1.8	-	mA
			OFF	DISABLE	1.1	-	
		24 MHz	ON	DISABLE	1	-	
			OFF	DISABLE	0.6	-	
		16 MHz	ON	DISABLE	0.75	-	
			OFF	DISABLE	0.5	-	
		8 MHz	ON	DISABLE	0.5	-	
			OFF	DISABLE	0.35	-	
		4 MHz	ON	DISABLE	0.4	-	
			OFF	DISABLE	0.35	-	
	LSI	32.768 kHz	ON	DISABLE	170	-	µA
			OFF	DISABLE	170	-	
		32.768 kHz	ON	ENABLE	95	-	
			OFF	ENABLE	96	-	

1. Data based on characterization results, not tested in production.

Table 5-9 Current consumption in Stop mode

Symbol	Conditions					Typ(1)	Max	Unit
	V_{CC}	V_{DD}	MR/LPR	LSI	Peripheral Clock			
I_{CC}(Stop)	2.0 to 5.5 V	1.2 V	MR	-	-	70	-	µA
		1.2 V	LPR	ON	RTC+IWDG+LPTIM	6	-	
					IWDG	6	-	
					LPTIM	6	-	
					RTC	6	-	
				OFF	No	6	-	
		1.0 V		ON	RTC+IWDG+LPTIM	4.5	-	
					IWDG	4.5	-	
					LPTIM	4.5	-	
					RTC	4.5	-	
				OFF	No	4.5	-	

1. Data based on characterization results, not tested in production.

5.3.5. Wakeup time from low-power mode

Table 5-10 Wake-up time from low-power mode

Symbol	Parameter[1]		Conditions		Typ[2]	Max	Unit
$t_{WUSLEEP}$	Wake-up from Sleep mode		-		10	-	CPU cycles
t_{WUSTOP}	Wake-up from Stop mode	MR	Run program in Flash, HSI (24 MHz) as system clock		3.5	-	μs
		LPR	Run program in Flash, HSI (24 MHz) as system clock	V_{DD}=1.2 V	6	-	μs
				V_{DD}=1.0 V	6	-	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Data based on characterization results, not tested in production.

5.3.6. High-speed internal (HSI) RC oscillator

Table 5-11 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	T_A = 25 °C, V_{CC} = 3.3 V	23.76[2]	24	24.24[2]	MHz
			21.89[2]	22.12	22.34[2]	
			15.84[2]	16	16.16[2]	
			7.92[2]	8	8.08[2]	
			3.96[2]	4	4.04[2]	
$\Delta_{Temp(HSI)}$	HSI frequency drift over temperature	V_{CC} = 2.0 to 5.5 V, T_A = 0 to 85 ℃	-2[2]	-	2[2]	%
		V_{CC} = 2.0 to 5.5 V, T_A = -40 to 105 ℃	-4[2]	-	2[2]	
f_{TRIM}[1]	HSI trimming step	-	-	0.1	-	%
D_{HSI}[1]	Duty cycle	-	45[1]	-	55[1]	%
$t_{Stab(HSI)}$	HSI stabilization time	-	-	2	4[1]	μs
$I_{CC(HSI)}$[2]	HSI power consumption	4 MHz	-	100	-	μA
		8 MHz	-	105	-	
		16 MHz	-	150	-	
		22.12 MHz, 24 MHz	-	180	-	

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.7. Low-speed internal (LSI) RC oscillator

Table 5-12 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	T_A = 25 °C, V_{CC} = 3.3 V	-3	-	3	%
$\Delta_{Temp(LSI)}$	LSI frequency drift over temperature	V_{CC} = 2.0 to 5.5 V, T_A = 0 to 85 °C	-10[2]	-	10[2]	%
		V_{CC} = 2.0 to 5.5 V, T_A = -40 to 105 °C	-20[2]	-	20[2]	
f_{TRIM}[1]	LSI trimming step	-	-	0.2	-	%
$t_{Stab(LSI)}$[1]	LSI stabilization time	-	-	150	-	μs
$I_{CC(LSI)}$[1]	LSI power consumption	-	-	210	-	nA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.8. Phase locked loop (PLL) characteristics

Table 5-13 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	T_A = 25 °C, V_{CC} = 3.3 V	16(1)	-	24(1)	MHz
f_{PLL_OUT}	PLL output clock	T_A = 25 °C, V_{CC} = 3.3 V	48	-	48	MHz
Jitter	Period jitter	-	-	-	0.3(1)	ns
t_{LOCK}	PLL lock time	f_{PLL_IN}=24 MHz	-	15	40(1)	μs

1. Guaranteed by design, not tested in production.

5.3.9. Memory characteristics

Table 5-14 Memory characteristics(2)

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog}	Page programming time	-	1.0	1.5	ms
t_{ERASE}	Page/sector/mass erase time	-	3.5	4.5	ms
I_{CC}	Page programming supply current	-	2.1	2.9	mA
	Page/sector/mass erase supply current	-	2.1	2.9	

1. Guaranteed by design, not tested in production.
2. When the program runs in SRAM and executes the Flash erase/write program, the CPU will stop working.

Table 5-15 Memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 to 85 ℃	100	kcycles
		T_A = 85 to 105 ℃	10	
t_{RET}	Data retention time	10 kcycles T_A = 55 °C	20	Years

1. Data based on characterization results, not tested in production.

5.3.10. EFT characteristics

Table 5-16 EFT characteristics

Symbol	Parameter	Conditions	Grade
EFT to Power	-	IEC61000-4-4	4 A

5.3.11. ESD & LU characteristics

Table 5-17 ESD & LU characteristics

Symbol	Parameter	Conditions	Typ	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	ESDA/JEDEC JS-001-2017	6	kV
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charged device model)	ESDA/JEDEC JS-002-2018	1	kV
$V_{ESD(MM)}$	Static Discharge Voltage (machine model)	JESD22-A115C	200	V
LU	Static Latch-up	JESD78E	200	mA

5.3.12. I/O port characteristics

Table 5-18 IO port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{CC} = 2.0 to 5.5 V	0.7*V_{CC}	-	-	V
V_{IL}	Input low level voltage	V_{CC} = 2.0 to 5.5 V	-	-	0.3*V_{CC}	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hys}(1)	I/O Schmitt trigger hysteresis	-	-	200	-	mV
	NRST Schmitt trigger hysteresis	-	-	300	-	mV
I_{lkg}	Input leakage current	-	-	-	1	μA
R_{PU}	Internal pull-up resistor	-	30	50	70	kΩ
R_{PD}	Internal pull-down resistor	-	30	50	70	kΩ
C_{IO}(1)	Pin capacitance	-	-	5	-	pF

1. Guaranteed by design, not tested in production.

Table 5-19 Output voltage characteristics

Symbol	Parameter(1)	Conditions	Min	Max	Unit
V_{OL}	COM IO output low level	I_{OL} = 8 mA, V_{CC} ≥ 2.7 V	-	0.4	V
		I_{OL} = 4 mA, V_{CC} = 1.8 V	-	0.5	
V_{OH}	COM IO output high level	I_{OH} = 8 mA, V_{CC} ≥ 2.7 V	V_{CC}-0.4	-	V
		I_{OH} = 4 mA, V_{CC} = 1.8 V	V_{CC}-0.5	-	

1. These I/O types refer to the terms and symbols defined by pins.
2. Data based on characterization results, not tested in production.

5.3.13. ADC characteristics

Table 5-20 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Analog power supply	-	2.0	-	5.5	V
I_{CC}	Consumption	@0.75 Msps	-	1.0	-	mA
C_{IN}(1)	Internal sampling and holding capacitor	-	-	5	-	pF
f_{ADC}	ADC clock frequency	V_{CC} = 2.0 to 2.3 V	1	4	6(2)	MHz
		V_{CC} = 2.3 to 5.5 V	1	8	12(2)	MHz
t_{samp}(1)	Sampling time	V_{CC} = 2.0 to 5.5 V	3.5	-	239.5	1/f_{ADC}
t_{samp_setup}(1)	V_{REFINT} sampling setup time	f_{ADC} = 12 MHz	20	-	-	μs
t_{conv}(1)	Total conversion time	-	-	12	-	1/f_{ADC}
t_{eoc}(1)	Conversion end time	-	-	0.5	-	1/f_{ADC}
DNL(2)	Differential nonlinearity error	-	-	±2	-	LSB
INL(2)	Integral nonlinearity error	-	-	±3	-	LSB
Offset(2)	Offset error	-	-	±2	-	LSB

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.14. Comparator characteristics

Table 5-21 Comparator characteris(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range	-	0	-	V_{CC}	V
V_{SC}	Offset voltage	-	-	±5	±10	mV
$I_{CC(SCALER)}$	Static consumption	-	-	0.8	1	μA
t_{START_SCALER}	Startup time	-	-	100	200	μs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{START}	Startup time	High-speed mode		-	-	5	µs
		Medium-speed mode		-	-	15	
t_D	Propagation delay	High-speed mode	200 mV step 100 mV over-drive	-	40	70	ns
			>200 mV step 100 mV over-drive	-	-	85	
		Medium-speed mode	200 mV step 100 mV over-drive	-	0.9	2.3	µs
			>200 mV step 100 mV over-drive	-	-	3.4	
V_{offset}	Offset voltage	-		-	±5	-	mV
V_{hys}	Hysteresis voltage	No hysteresis		-	0	-	mV
		With hysteresis		-	20	-	
I_{CC}	Operating current	Medium-speed mode	Static	-	7	-	µA
			With 50 kHz and ±100 mv overdrive square signal	-	8	-	
		High-speed mode	Static	-	250	-	
			With 50 kHz and ±100 mv overdrive square signal	-	250	-	

1. Guaranteed by design, not tested in production.

5.3.15. Temperature sensor characteristics

Table 5-22 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±2	±5	℃
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/℃
V_{25}	Voltage at 25 ℃ (±5 ℃)	0.742	0.76	0.785	V
t_{START}(1)	Start up time entering in continuous mode	-	70	120	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	20	-	-	µs

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.16. Embedded voltage reference characteristics

Table 5-23 Embedded voltage reference characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	1.17	1.2	1.23	V
$t_{start\_vrefint}$	Start time of V_{REFINT}	-	10	15	µs
T_{coeff}	Temperature coefficient of V_{REFINT}	-	-	100(1)	ppm/℃
I_{vcc}	Current consumption from V_{CC}	-	12	20	µA

1. Guaranteed by design, not tested in production.

5.3.17. Timer characteristics

Table 5-24 Timer characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.833	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48 MHz	-	24	
Res_{TIM}	Timer resolution time	TIM1/3/14/16/17	-	16	bit
$t_{COUNTER}$	16-bit counter internal clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.020833	1365	μs

Table 5-25 LPTIM characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PRESC[2:0]	Min	Max	Unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.9456	
/8	3	0.2441	15997.3376	
/16	4	0.4883	32001.2288	
/32	5	0.9766	64002.4576	
/64	6	1.9531	127998.3616	
/128	7	3.9063	256003.2768	

Table 5-26 IWDG characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PR[2:0]	Min	Max	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 5-27 WWDG characteristics (timeout period at 48 MHz PCLK)

Prescaler	WDGTB[1:0]	Min	Max	Unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	
4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

5.3.18. Communication interfaces

5.3.18.1. I²C interface characteristics

I²C interface meets the requirements of the I²C bus specification and reference manual:

- Standard-mode (Sm): 100 kHz
- Fast-mode (Fm): 400 kHz

I²C SDA and SCL pins have analog filtering, see table below.

Table 5-28 I²C filter characteristics

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter (Spikers shorter than the limiting duration are suppressed)	50	260	ns

5.3.18.2. SPI characteristics

Table 5-29 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	12	MHz
		Slave mode	-	12	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4 * T_{pclk}	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2 * T_{pclk} + 10	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, presc = 4	T_{pclk} * 2 - 2	T_{pclk} * 2 + 1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode, presc = 4	T_{pclk} + 5(1)	-	ns
		Slave mode, presc = 4	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	ns
$t_{h(SI)}$		Slave mode	T_{pclk} + 5	-	
$t_{a(SO)}$	Data output access time	Slave mode, presc = 4	0	3 * T_{pclk}	ns
$t_{dis(SO)}$	Data output access time	Slave mode	2 * T_{pclk} +5	4 * T_{pclk} +5	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge) presc = 4	0	1.5 * T_{pclk}(2)	ns
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	ns
$t_{h(SO)}$	Data output hold time	Slave mode, presc = 4	0(3)	-	ns
$t_{h(MO)}$		Master mode	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

1. The Master generates a 1 PCLK receive control signal before the receive edge.
2. Slave defines 1.5 PCLK based on the maximum 1 PCLK delay on the SCK transmission edge, considering IO delay, etc.
3. The Slave updates the data before the transmit edge if the SCK duty cycle sent by the Master is wide between the receive edge and the transmit edge.

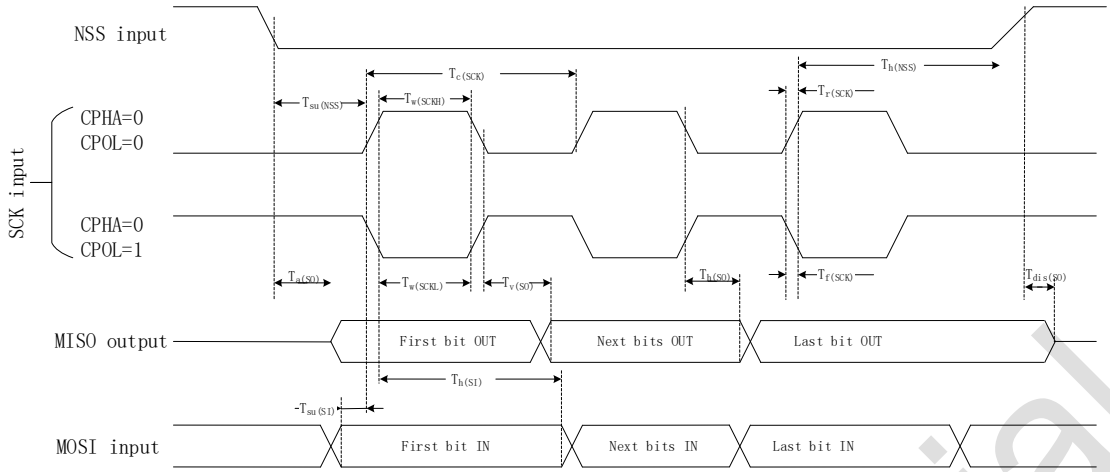


Figure 5-1 SPI timing diagram – Slave mode and CPHA=0

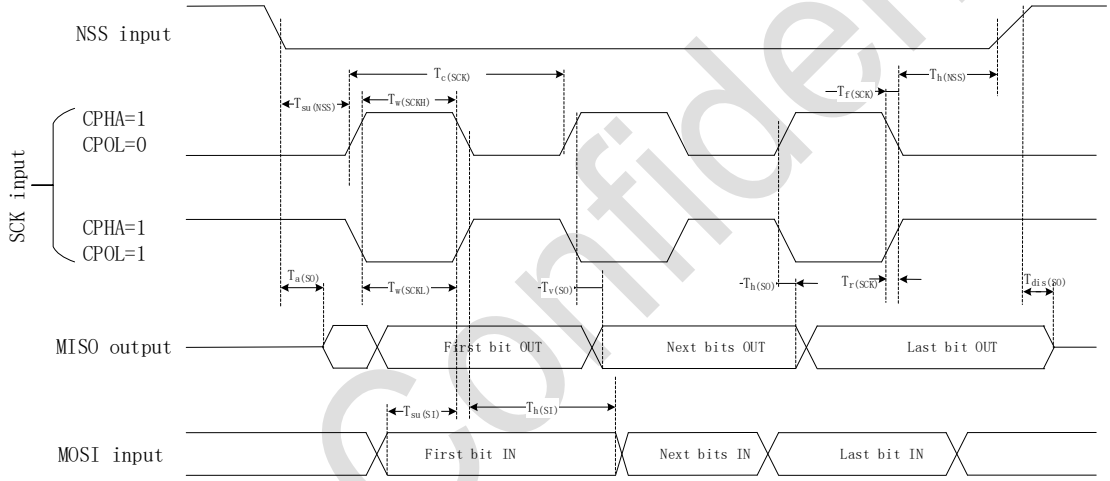


Figure 5-2 SPI timing diagram – Slave mode and CPHA=1

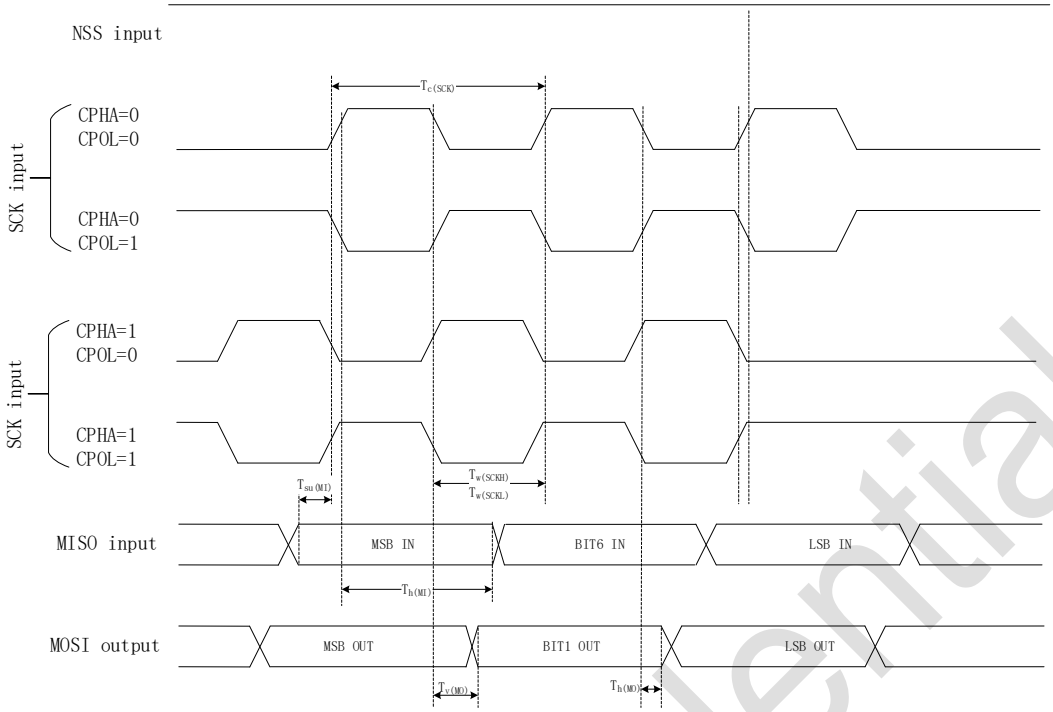


Figure 5-3 SPI timing diagram – Master mode

5.4. Multifunction gate driver electrical characteristics

The gate driver is a three-phase brushless gate driver that can drive N+N MOS and operate at a power supply voltage of 5.5 to 18 V. The gate driver has a built-in 50 mA LDO that can provide power to the MCU or other devices.

The gate driver features built-in shoot-through prevention and a 250 ns dead time to prevent shoot-through of the driven high- and low-side MOSFETs, effectively protecting the power devices.

The gate driver also features a built-in input voltage V_{IN}/V_B under-voltage lockout (UVLO) function, which can effectively prevent the power devices from operating at excessively low voltages.

5.4.1. Drive logic control

The gate driver features input/output high- and low-side channel matching. The HINx input channel is active high and controls the high-side HOx output; the LINx input channel is active high and controls the low-side LOx output.

Table 5-30 Logic control truth table

HINx	LINx	HOx	LOx
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

5.4.2. Switching time

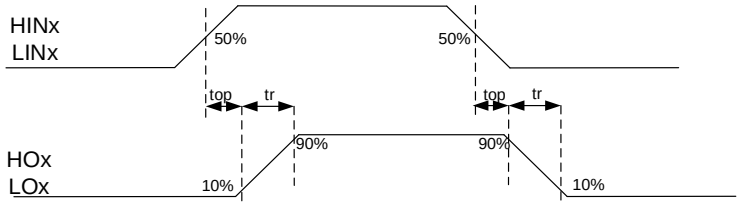


Figure 5-4 Switching time

5.4.3. Shoot-through protection

The gate driver is internally designed with a dedicated protection circuit to prevent power tube shoot-through, which can effectively prevent shoot-through damage to the power tubes caused by interference with the high-side and low-side input signals.

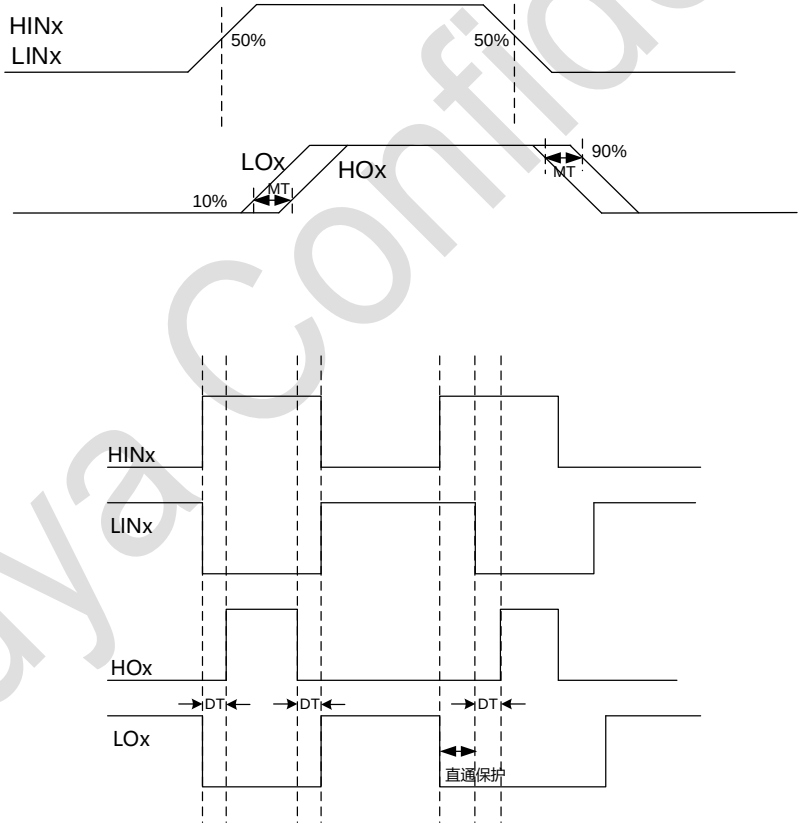


Figure 5-5 Shoot-through protection

5.4.4. Dead time function

A fixed dead time protection circuit is set inside the gate driver. During the dead time, both the high-side and low-side outputs are set to a low level. The set dead time must ensure that one power de-

vice is turned off before the other is turned on, effectively preventing shoot-through between the upper and lower power devices. If the logic input has an external dead time set and this time is greater than the chip's internal dead time (250 ns), the external logic input's dead time is used as the chip's dead time; if the logic input has an external dead time set and this time is less than the chip's internal dead time (250 ns), the chip's internal dead time (250 ns) shall prevail.

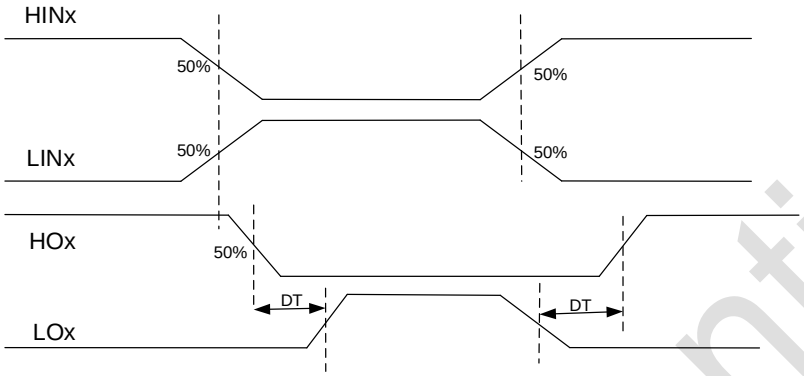
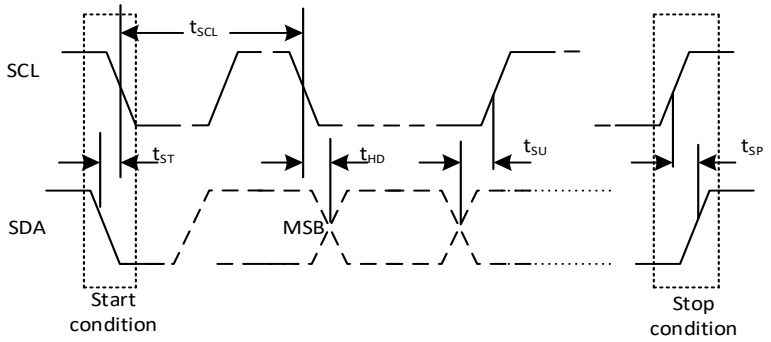


Figure 5-6 Dead time function

5.4.5. I²C interface and register definitions

Note: Unless otherwise specified, T_A = 25 °C.

Parameter	Test conditions	Min	Typ	Max	Unit
SCL, SDA input low	V_{LDO} = 5.0 V	-	-	1.2	V
SCL, SDA input high	V_{LDO} = 5.0 V	3.8	-	-	V
SDA leakage current	SDA = V_{LDO}	-	-	1	μA
SDA output low	I_{OL} = 1 mA	-	-	0.3	V
SCL clock frequency, f_{SCL}	-	0	-	100	kHz
SCL low period, t_{LOW}	-	0.5	-	-	μs
SCL high period, t_{HIGH}	-	0.5	-	-	μs
SDA data setup time, t_{SU}	-	100	-	-	ns
SDA data hold time, t_{HD}	-	100	-	-	ns
Start setup time, t_{ST}	For start condition	300	-	-	ns
Stop setup time, t_{SP}	For stop condition	300	-	-	ns
Capacitance on SCL or SDA pin	-	-	-	10	pF
SDA fall time, t_{OF}	Device requirement	-	-	100	ns
Pulse width of spikes must be suppressed on SCL and SDA	-	-	0	50	ns



1. Read/write byte length is limited to 1 byte
2. SDA/SCL require external pull-up resistors, SCL frequency below 100 kHz (TBD)
3. I²C address (7 bits): 0b 0101 010X (X = 0 write; X = 1 read)
4. Method to exit suspend: Master sends (Start + 9 Times CLK + Stop)

5.4.6. I²C transmission

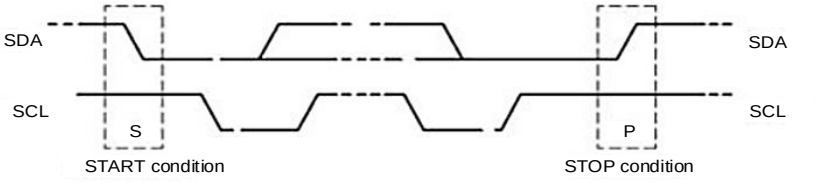


Figure 5-7 Start and stop conditions

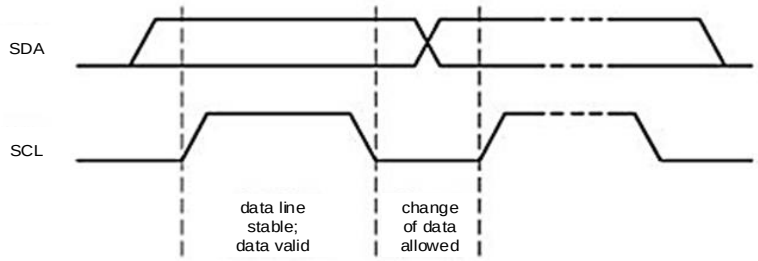


Figure 5-8 I²C bus timing diagram

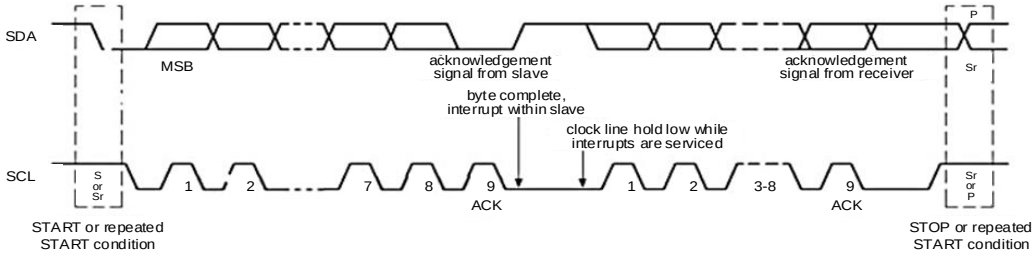


Figure 5-9 I²C bus timing diagram

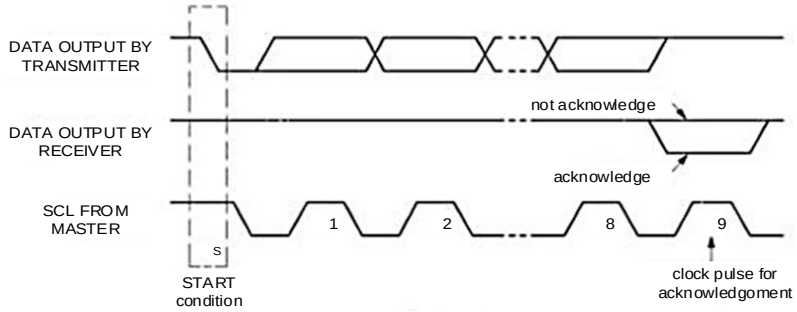


Figure 5-10 I²C bus data transmission

5.4.7. Write command format

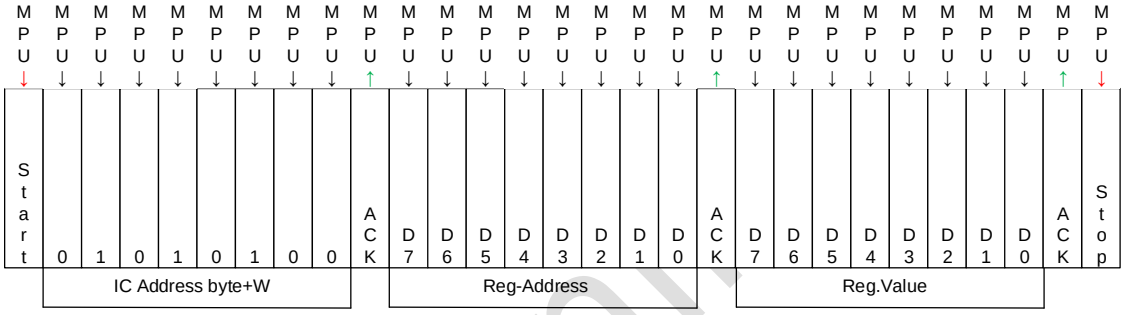


Figure 5-11 Write command format

5.4.8. Read command format

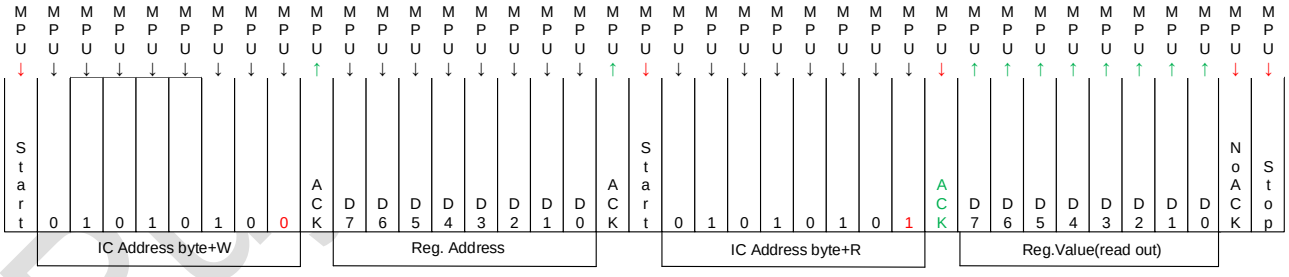


Figure 5-12 Read command format

5.4.9. Register definitions

Table 5-31 Register definitions

Register Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
00H	Isense_bias[1:0]		IBUS_Gain[2:0]			IUV_Gain[2:0]			D3H
01H	en_sense_vdd	IBUS_cmp_sel	dac_sel[5:0]						4AH
02H	0	1	en_osc_vdd	en_zero_vdd	Zero_res[1:0]		Zero_bias [1:0]		69H

Table 5-32 Default values

Name	Bit	Default
Isense_bias	[1:0]	11
IBUS_Gain	[2:0]	010
IUVGain	[2:0]	011
en_sense_vdd	-	0
IBUS_cmp_sel	-	1
dac_sel	[5:0]	001010
r2_76(reserved)	[1:0]	01
en_osc_vdd	-	1
en_zero_vdd	-	0
Zero_res	[1:0]	10
Zero_bias	[1:0]	01

5.4.10. Bus current sensing

IBUS_OUT output voltage = V_{LDO} * Bias + IBUS * RBUS * IBUS_Gain

Where IBUS is the motor bus current, RBUS is the bus current sensing resistor in the figure above, and IBUS_Gain[2:0] is defined as:

IBUS_Gain[2:0]	Bias	IBUS_Gain
000 b	1/5	1
001 b	1/5	2
010 b	1/5	4
011 b	1/5	8
100 b	0	2
101 b	0	3
110 b	0	5
111 b	0	9

5.4.11. Bus overcurrent protection

Vref (DAC output voltage) = 50 mV * dac_sel

The DAC register dac_sel[5:0] is defined as:

dac_sel[5:0]	dac_sel	Vref
000 000 b	0	0
000 001 b	1	50 mV
000 010 b	2	100 mV
000 011 b	3	150 mV
……	……	……
110 111 b	55	2.75 V
……	……	……
111 111 b	63	3.15 V

When the bus current exceeds the limit, causing the voltage to exceed the Vref setting, OC transitions from high to low, triggering protection and requesting an MCU interrupt;

1. It is generally not recommended to set the Vref voltage too high, such as exceeding 2.0 V;
2. If a register error occurs due to interference, the error correction mechanism will also pull OC_OUT low to trigger protection and request an MCU interrupt.

5.4.12. Zero-crossing detection

Three built-in comparators perform zero-crossing detection with the three-phase input voltages respectively, via a virtual neutral point created by internal 250 kΩ resistors. The phase voltage division ratio can be configured into four ratio modes via I²C. The three-phase voltages are directly routed to the comparators from the bootstrap circuit VS ports internally, eliminating the need for separate external routing. The internal circuit block diagram is as follows:

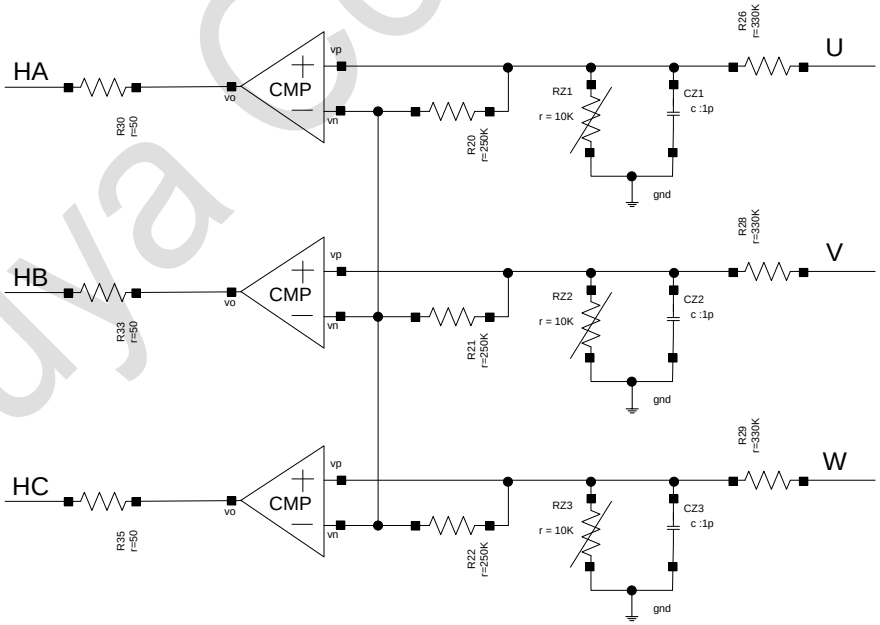


Figure 5-13 Internal circuit block diagram for zero-crossing detection

The Zero_res[1:0] register is defined as:

Zero_res[1:0]	RZ1/2/3
00 b	100k

Zero_res[1:0]	RZ1/2/3
01 b	50k
10 b	25k
11 b	12.5k

5.4.13. Absolute maximum ratings

Table 5-33 Absolute maximum ratings

Symbol	Descriptions	Parameter range	Unit
V_{IN}	Low-side supply voltage	-0.3 to 18	V
V_{Bx}	High-side floating supply	-0.3 to 40	V
V_{Sx}	High-side floating reference ground	V_{Bx}-18 to V_{Bx}+0.3	V
V_{LDO}	LDO output voltage range	-0.3 to 5.5	V
$V_{HIN1,2,3}$	High-side control input voltage	-0.3 to V_{LDO}+0.3	V
$V_{LIN1,2,3}$	Low-side control input voltage	-0.3 to V_{LDO}+0.3	V
COMPx	Comparator supply voltage	-0.3 to V_{LDO}+0.3	V
$V_{HO1,2,3}$	High-side gate Driver Output Voltage	V_{Sx}-0.3 to V_{Bx}+0.3	V
$V_{LO1,2,3}$	Low-Side Gate Driver Output Voltage	-0.3 to V_{IN}+0.3	V
OPAO/OPAxO	Current sense op-amp output voltage range	-0.3 to V_{LDO}+0.3	V
OPAI+/OPAxI, OPAI-/IGND	Current sense op-amp input voltage range	-0.3 to V_{LDO}+0.3	V
OC	Current short-circuit protection comparator output voltage range	-0.3 to V_{LDO}+0.3	V

5.4.14. Recommended operating conditions

Table 5-34 Recommended operating conditions

Symbol	Descriptions	Min	Typ	Max	Unit
V_{IN}	Low-side supply voltage	5.5	12	18	V
V_{Bx}	High-side floating absolute voltage	V_{Sx}+5.5	-	40	V
V_{Sx}	High-side floating offset voltage	-0.3	-	24	V
V_{LDO}	LDO Output Voltage Range	-	5.0	-	V
$V_{HIN1,2,3}$	High-Side Control Input Voltage	0	-	V_{LDO}	V
$V_{LIN1,2,3}$	Low-Side Control Input Voltage	0	-	V_{LDO}	V
COMPx	Comparator supply voltage	0	V	V_{LDO}	V
OPAO/OPAxO	Current sense op-amp output voltage range	0	-	V_{LDO}	V
OPAI+/OPAxI, OPAI-/IGND	Current sense op-amp input voltage range	0	-	V_{LDO}	V
OC	Current short-circuit protection comparator output voltage range	0	-	V_{LDO}	V
T_A	Operating temperature	-40	-	105	℃
f_{PWM}	PMW frequency	0	-	200	kHz

5.4.15. Electrical characteristics table

Note: Unless otherwise specified, T_A = 25 ℃, V_{IN} = 12 V, V_{Sx} = V_{GND}.

Table 5-35 Electrical characteristics table

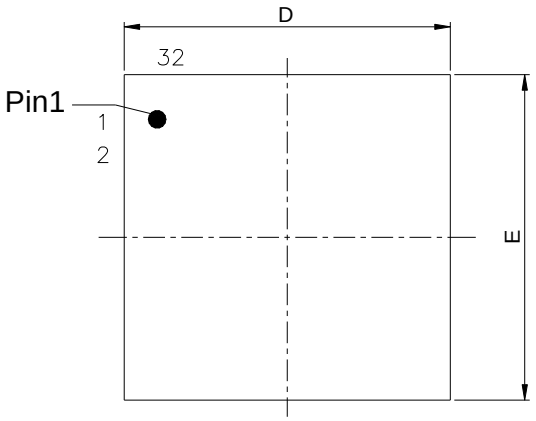
Symbol	Descriptions	Min	Typ	Max	Unit
Electrical characteristics					
I_{VIN}	V_{IN} operating current, H_{INX}=L_{INX}=20 kHz	-	600	-	μA
I_{VINQ}	V_{IN} quiescent current, H_{INX}=L_{INX}=0 V	-	300	-	μA
I_{VBS}	V_{BS} operating current, H_{INX}=L_{INX}=20 kHz	-	800	-	μA
I_{VBSQ}	V_{BS} quiescent current, H_{INX}=L_{INX}=0 V	-	40	-	μA
V_{SN}	V_S static negative voltage	-	-6	-	V
LDO					
V_{LDO}	LDO output voltage, I_{OUT}=1 mA, V_{IN}=12V	4.75	5	5.25	V
I_{OUT}	LDO output current capability, V_{IN}=12 V, V_{OUT}>95%*V_{LDO}	-	-	50	mA
I_{LDOQ}	LDO quiescent current, I_{OUT}=0 mA	-	20	-	μA
Load regulation	1 mA<I_{OUT}<50 mA	-	15	20	mV
Line regulation	7 V<V_{VIN}<20 V	-	0.1	0.2	%/V
Three-phase gate driver					
V_{IL}	Logic input low voltage	-	-	0.4/0.8	V
V_{IH}	Logic input high voltage	1.6/2.0	-	-	V
V_{UVLO_F}	V_{IN}/V_B undervoltage lockout hysteresis	-	4	-	V
V_{UVLO_R}	V_{IN}/V_B undervoltage lockout hysteresis	-	4.5	-	V
V_{UVLO_HYS}	V_{IN}/V_B undervoltage lockout hysteresis	-	0.5	-	V
I_{LK}	Floating supply leakage current V_{Bx}=V_{Sx}=150 V	-	0.1	5	μA
I_{LIN+}	LIN high-level input bias current V_{LIN}=5 V	-	25	40	μA
I_{LIN-}	LIN low-level input bias current V_{LIN}=0 V	-	-	1	μA
I_{HIN+}	HIN high-level input bias current V_{HIN}=5 V	-	25	40	μA
I_{HIN-}	HIN low-level input bias current V_{HIN}=0 V	-	-	1	μA
Rpd	Weak pull-down equivalent resistor	-	200	-	kΩ
V_{OL}	Low-level output voltage I_{OUT}=-100mA, V_{IN}=12 V	-	0.3	0.45	V
V_{OH}	High-level output voltage I_{OUT}=100mA, V_{IN}=12 V	-	10	12	V
I_{DRIVEP}	IO output current	-	800	-	mA
I_{DRIVEN}	IO output current	-	-800	-	mA
T_{PW_MIN}	Minimum input pulse width	-	70	-	ns
t_{DT}	Dead time	-	250	-	ns
t_r	Output rise time, C_L=1000 pF	-	50	100	ns
t_f	Output fall time, C_L=1000 pF	-	50	100	ns
t_{on}	Output rising edge propagation time	-	300	450	ns
t_{OFF}	Output falling edge propagation time	-	100	160	ns
MT	High and low side delay matching	-	-	30	ns
Op-amp					

Symbol	Descriptions	Min	Typ	Max	Unit
V_{OP}	Op-amp operating voltage	-	V_{LDO}	-	V
I_{SUP}	Op-amp operating current	-	100	-	μA
V_{OFFSET}	Offset voltage	-	5	-	mV
VC_{RANGE}	Input voltage range	0.2	-	V_{OP}-0.2	V
I_{IN}	Low input bias current	-	-	1	μA
I_{SOURCE}	Output current	1000	-	-	μA
I_{SINK}	Output current	1000	-	-	μA
V_{SW}	Output voltage swing	0	-	V_{OP}	V
Av	Open-loop gain R_L=100 kΩ	-	80	-	dB
BW	Bandwidth C_L=30 pF	-	10	-	MHz
PSRR	Power supply rejection ratio	60	90	-	dB
SR	Op-amp slew rate C_L=30 pF	5	-	-	V/μS

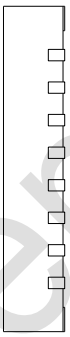
6. Package information

6.1. QFN32(4*4) package size

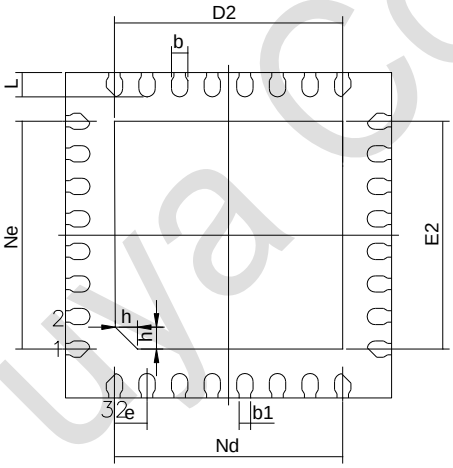
TOP VIEW



SIDE VIEW



BOTTOM VIEW



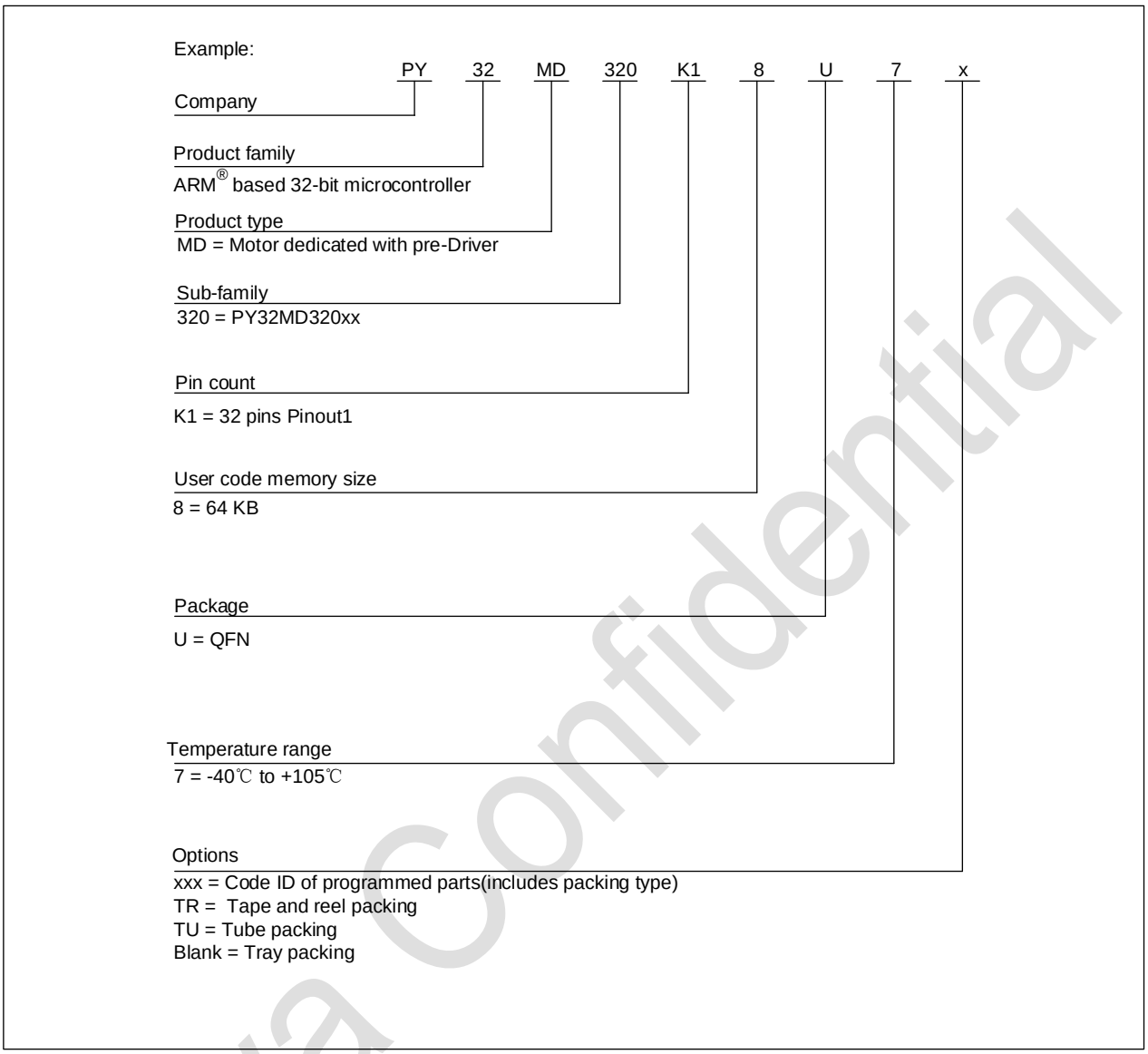
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c	0.180	0.200	0.250
D	3.900	4.000	4.100
D2	2.700	2.850	3.000
E	3.900	4.000	4.100
E2	2.700	2.850	3.000
e	0.400BSC		
Nd	2.800BSC		
Ne	2.800BSC		
b1	0.140REF		
L	0.200	0.300	0.400
h	0.300	0.350	0.400

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN32L 4X4X0.75-0.4PITCH POD	QRPD-0060	1.0

7. Ordering information



8. Version history

Version	Date	Descriptions
V1.0	2023.12.01	Initial version
V1.1	2023.12.15	Updated Section 5.4 title
V1.2	2024.01.29	Junction temperature range: -40 to 110℃ adjusted to -40 to 125℃
V1.3	2024.11.15	1. MCU operating voltage range adjusted: 2.0 to 5.5 V 2. Updated the measured parameters
V1.4	2026.06.09	1. Added note on Flash erase/write restrictions 2. Updated characteristic parameters of temperature sensor

Puya Semiconductor Co., Ltd.